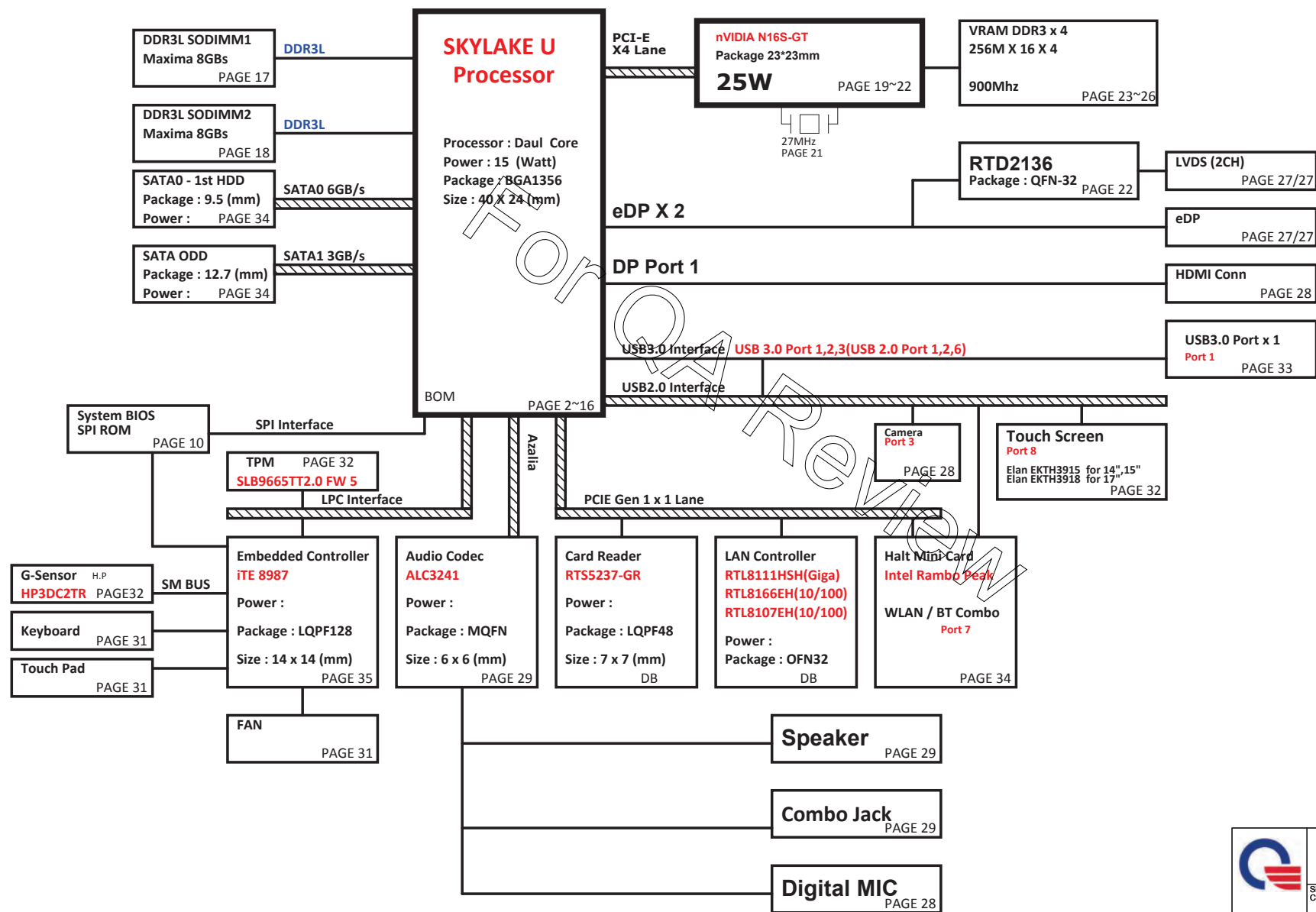


# DIS (14" / 15" / 17") Chocolate

## Intel SKYLAKE ULT Platform Block Diagram

PCB 6L STACK UP

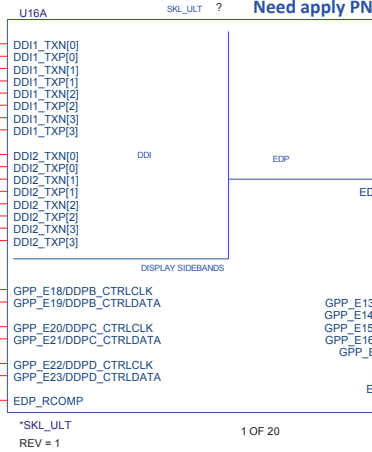
LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2(Low)  
LAYER 5 : SVCC  
LAYER 6 : BOT



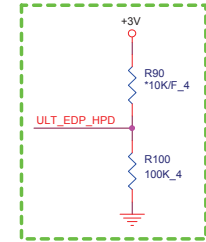
+3V 4,10,11,12,13,14,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44  
+1.0V 4,6,16,32,35,40  
+VCCSTPLL 4,5,6,9,40,41

## HDMI

28 IN\_D2# IN\_D2# E55  
28 IN\_D2 IN\_D2 F55  
28 IN\_D1# IN\_D1# F58  
28 IN\_D1 IN\_D1 F53  
28 IN\_D0# IN\_D0# G53  
28 IN\_D0 IN\_D0 F56  
28 IN\_CLK# IN\_CLK# F56  
28 IN\_CLK IN\_CLK G56



Reserve EDP\_HPD opposites circuit!

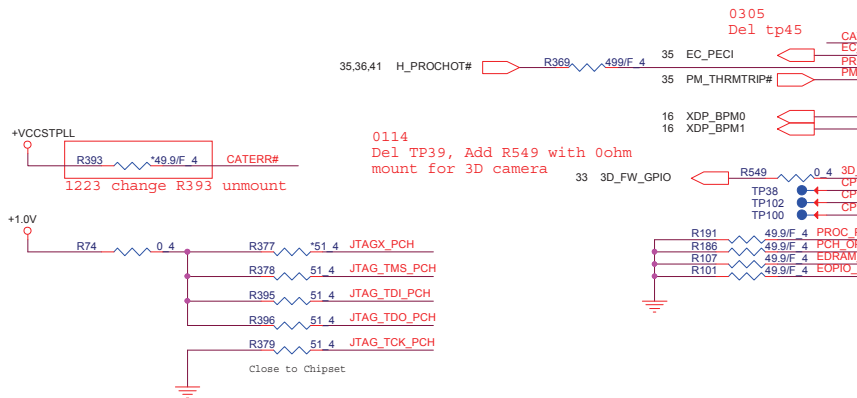


1223 Del R93, R102

1225 DDPC\_CTRLCLK and DDPC\_CTRLCLK reserve TP

eDP\_CMPIO and ICMPIO signals should be shorted near balls and routed with typical impedance &lt;25 mohms

1218 change R96 connection from +1.0V to +VCCIO



Close to EC

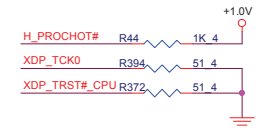
PM\_THRMTRIP# R392 1K 4 +VCCSTPLL

Processor pull-up (CPU)  
TO BE REPLACED WITH 1K OHMS FOR SKL  
470 OHM IS FOR I/P

PLACE NEAR CPU

XDP\_TMS\_CPU R380 51.4  
XDP\_TDI\_CPU R376 51.4  
XDP\_TDO\_CPU R367 51.4

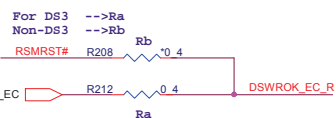
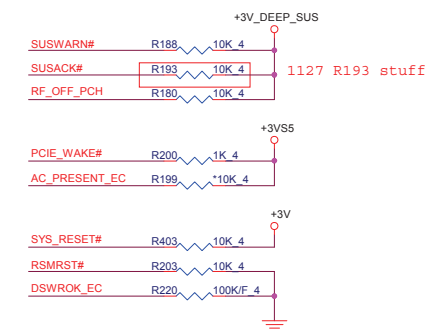
1218 Unmount R380, R367



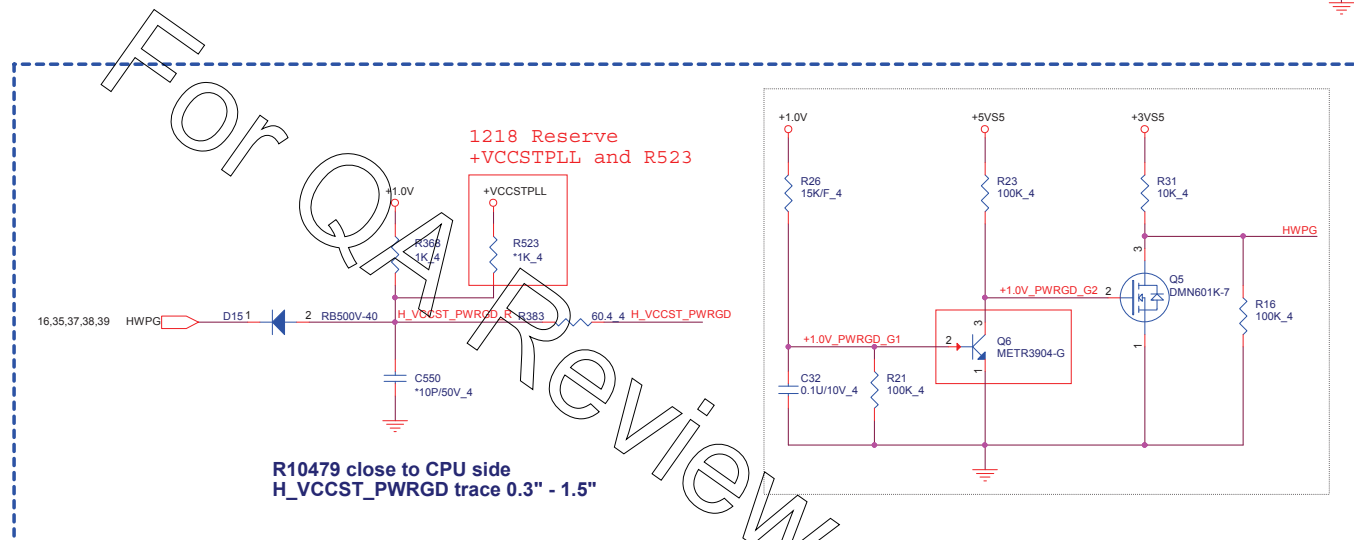
**PROJECT :Y11X-6L**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>02 - SKYPAKE 1/20(eDP/DDI)</b>	Rev 1A
Date: Wednesday, May 06, 2015	Sheet 2 of	49



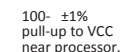



PLTRST# 16,19,30,32,34,35



**PROJECT :Y11X-6L**  
Quanta Computer Inc.

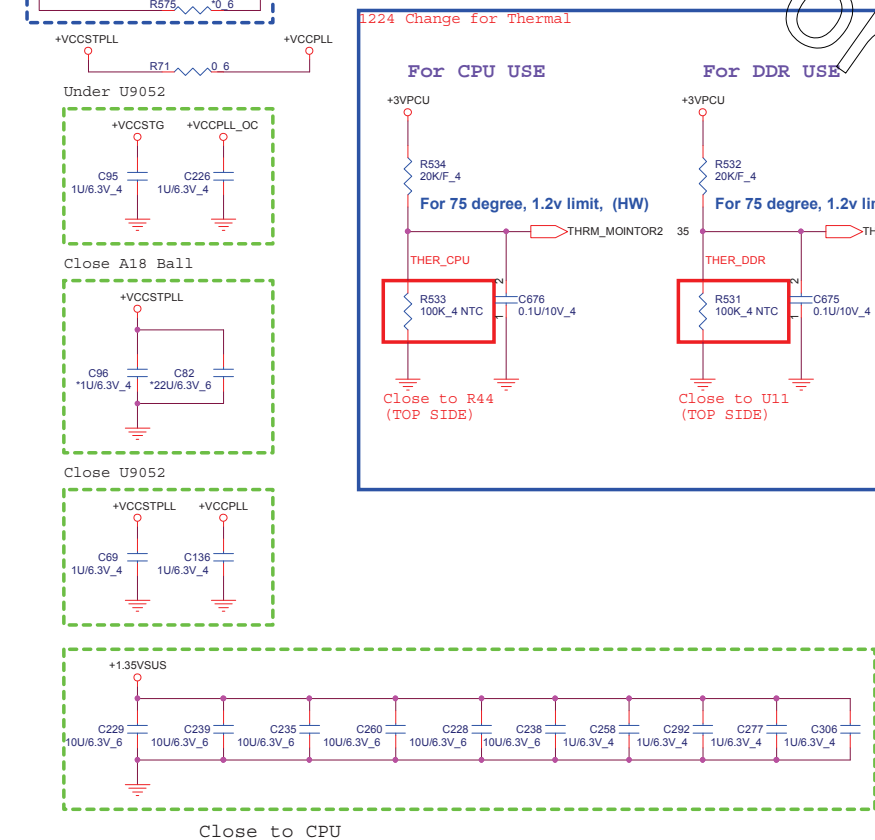
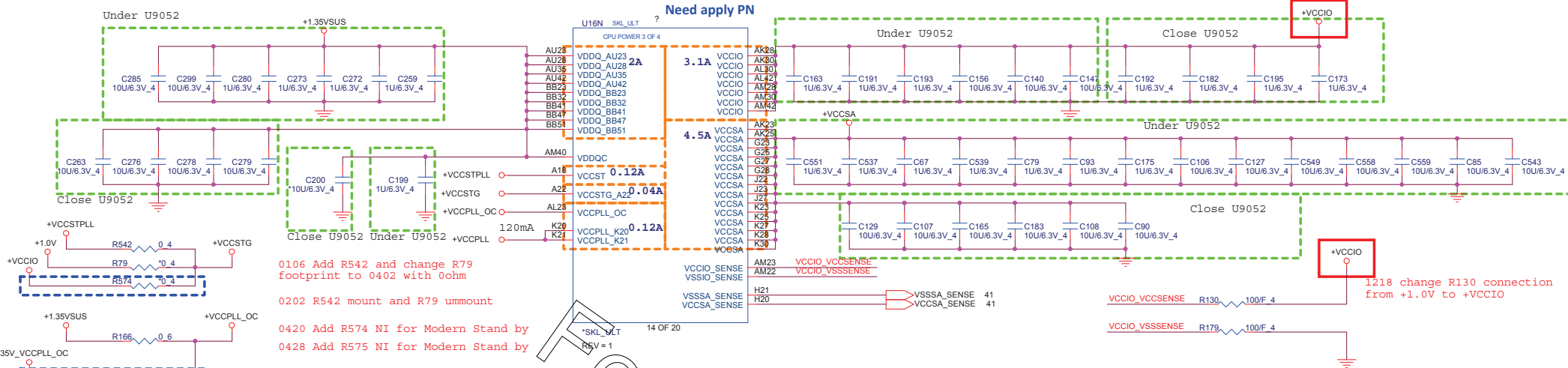
Size Custom	Document Number <b>04 -- SKYPAKE 5/20(Power Manger)</b>	Rev 1A
Date: Wednesday, May 06, 2015	Sheet 4 of	49



	<b>PROJECT :Y11X-6L</b> Quanta Computer Inc.		
	Size Custom	Document Number <b>05 -- SKYPAKE 6/20 (POWER-1)</b>	Rev 1A
	Date: Wednesday, May 06, 2015	Sheet	5 of 49



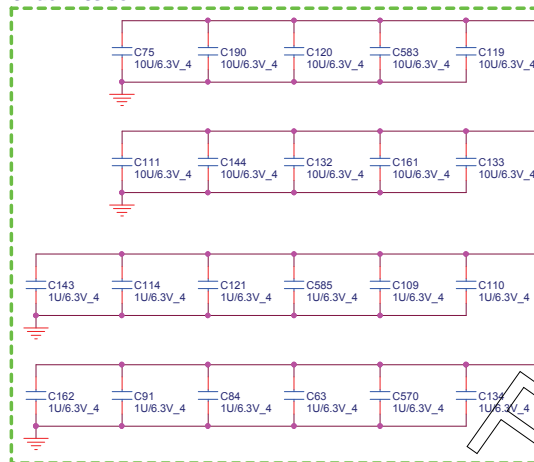
Input	Pin Numbers
+VCCSTPLL	2,4,5,9,40,41
+VCCSA	41,42
+1.35VSUS	3,17,18,38,40,46
+1.0V_DEEP_SUS	9,13,15,16,39,40
-1.0V	2,4,16,32,35,40
+3VPCU	13,30,31,32,33,34,35,36,37



Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_LPS</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

+VCCGT 41  
+VCC\_CORE 5,41  
+1.35VSUS 3,6,17,18,38,40,46

Under U9052



U16M SKL\_ULT ? Need apply PN

31A

41 VCCGT\_SENSE  
41 VSSGT\_SENSE

U16M SKL\_ULT ? Need apply PN

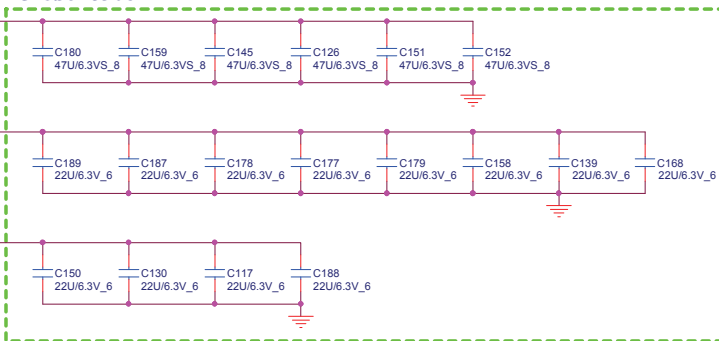
CPU POWER 2 OF 4

31A

AK42  
AK43  
AK44  
AK45  
AK46  
AK47  
AK48  
AK49  
AK50  
AK51  
AK52  
AK53  
AK54  
AK55  
AK56  
AK57  
AK58  
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AK95  
AK96  
AK97  
AK98  
AK99  
AK100

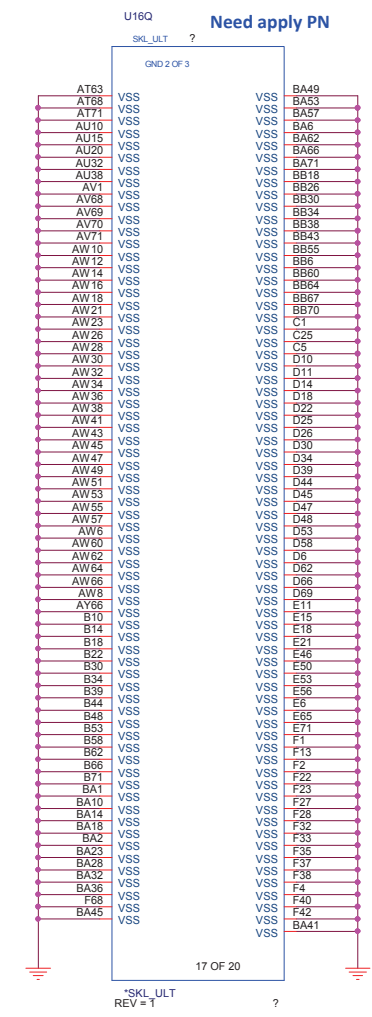
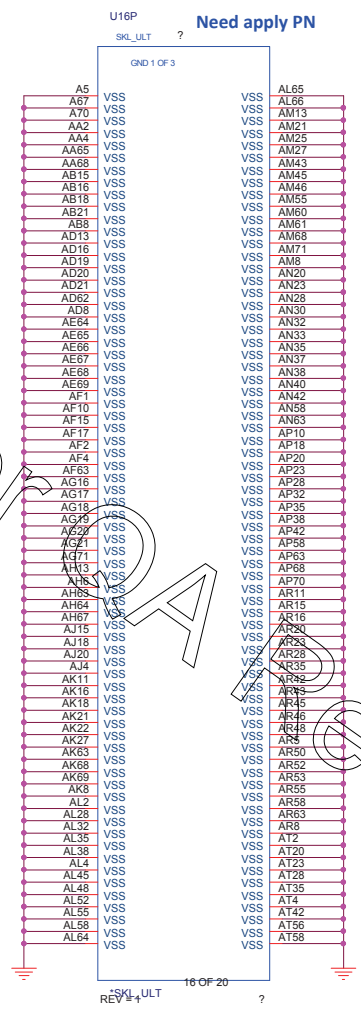
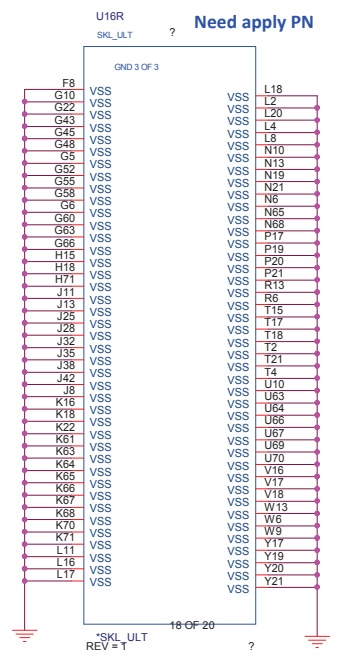
+VCCGT

Close U9052

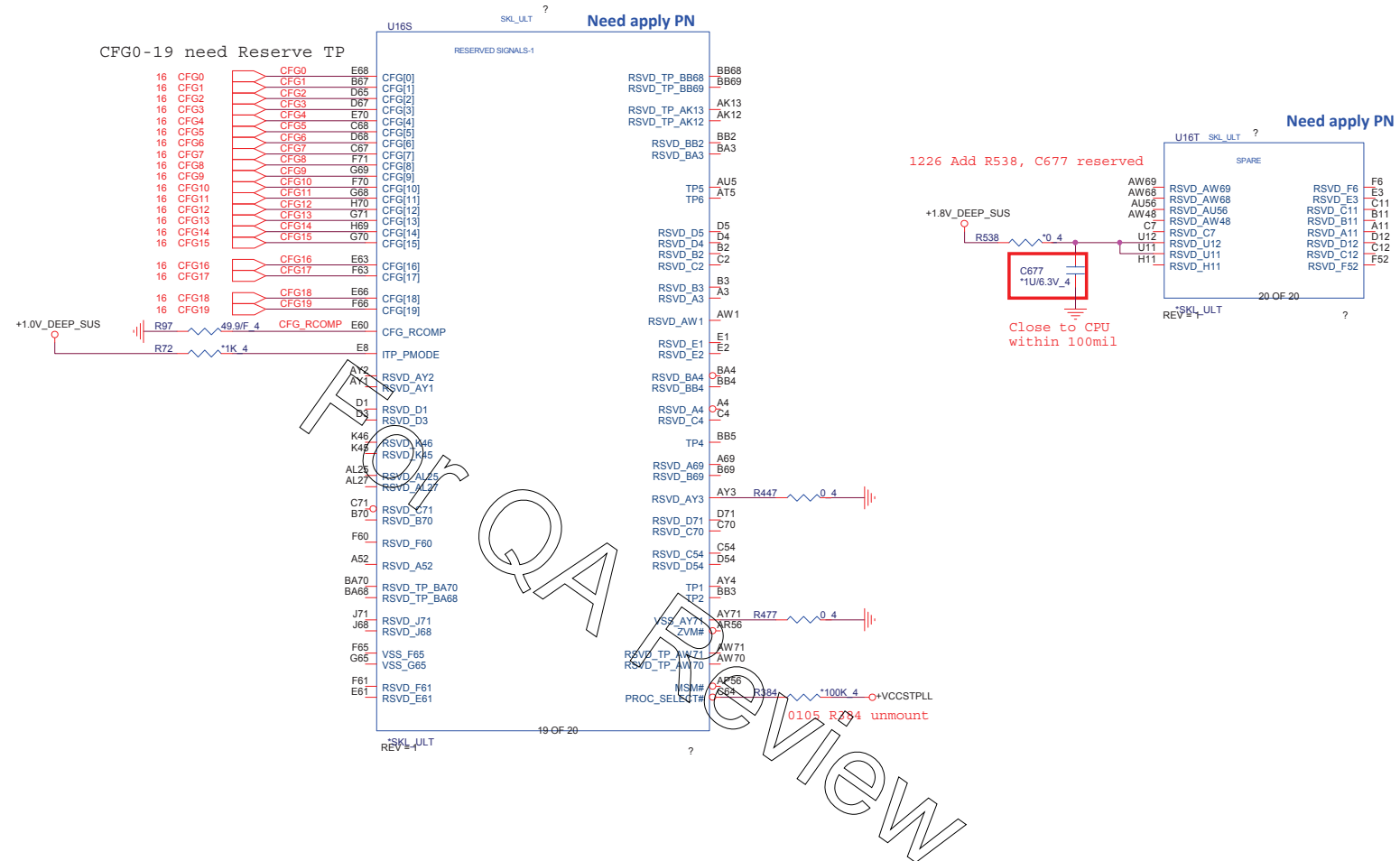


\*SKL\_ULT 13 OF 20  
REV = 1

Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTX</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_LPB</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCIOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed







## Processor Strapping

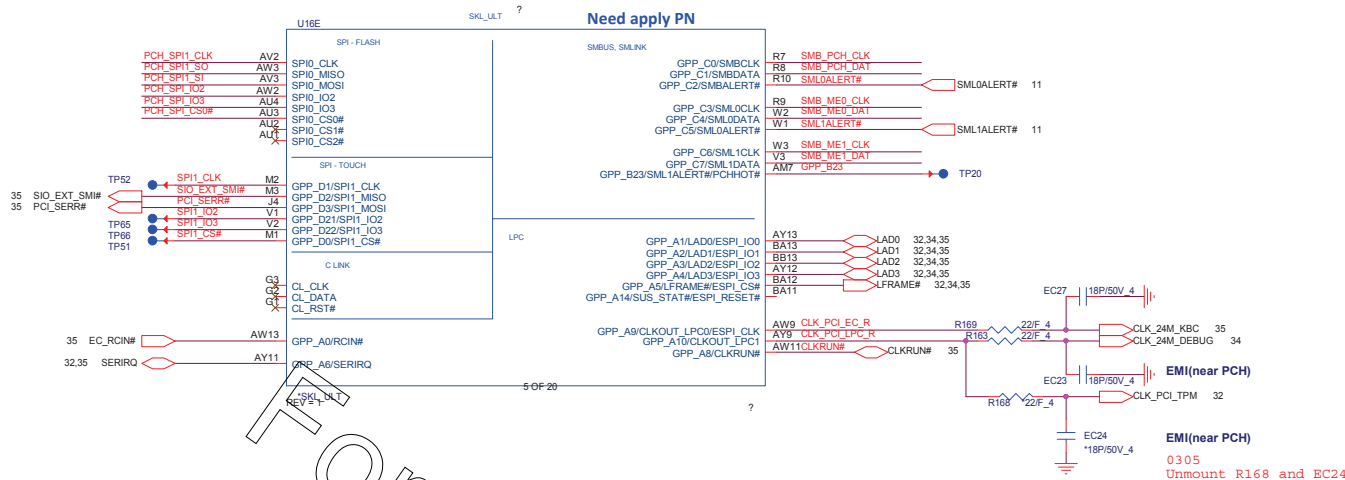
The CFG signals have a default value of '1' if not terminated on the board.

Processor Debugging			
	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	

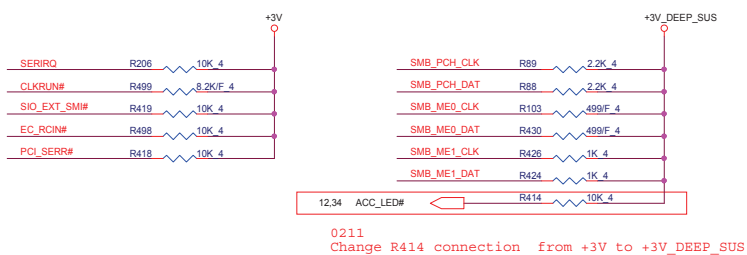


**PROJECT :Y11X-6L**  
Quanta Computer Inc.

Size Custom	Document Number <b>9 -- SKYPAKE 12/20 (RSV-1)</b>	Rev 1A
Date: Wednesday, May 06, 2015	Sheet	9 of 49

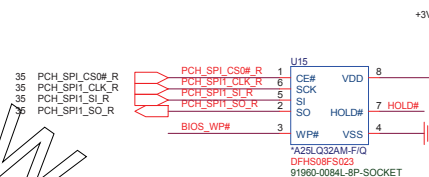


PCH SPI ROM(CLG)



Vender	Size	P/N
EON	8MB	AKE3EZNOQ01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFPNO07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGNOQ01 (GD25B64BSIGR)
Socket		DFHS08FS023

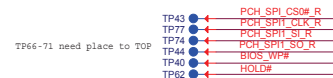
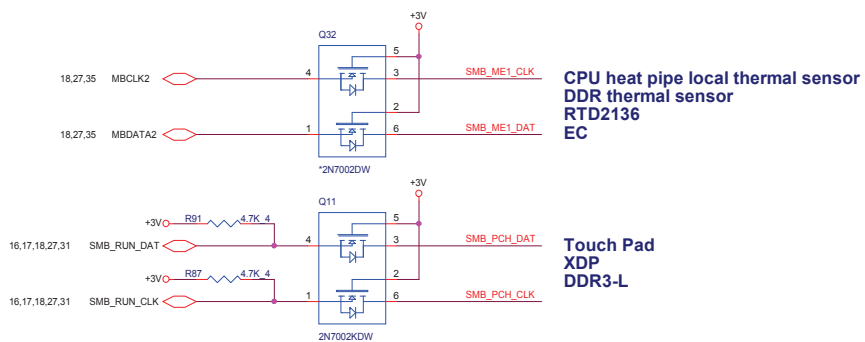
### 4M SPI ROM Socket



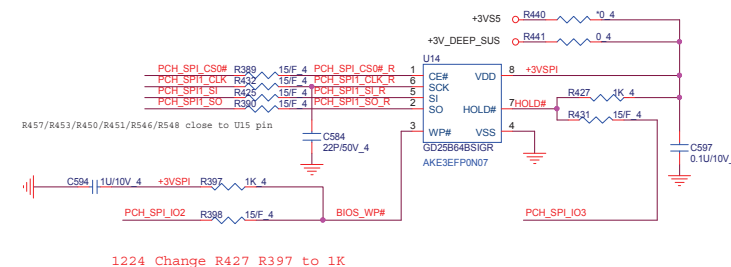
```
0211
Change mount U14, unmount U15
```

U23&U24 footprint 要重疊

### SMBus/Pull-up(CLG)



### PCH SPI ROM(CLG)



**PROJECT :Y11X-6L**  
Quanta Computer Inc.

Size Custom	Document Number <b>10 -- SKYPAKE 14/20(SPI/LPC/SMBUS)</b>	Rev 1
Date: Wednesday, May 06, 2015	Sheet 10 of 49	

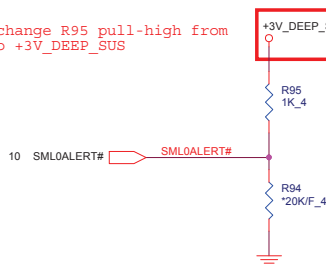
# Functional Strap Definitions

**DESIGN NOTE:**  
WEAK PULL UP RESISTOR PRESENT ON THIS NET

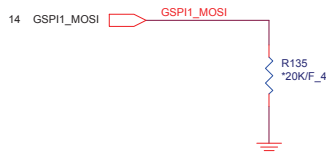


**TOP SWAP OVERRIDE**  
HIGH - TOP SWAP ENABLE  
LOW-DISABLED  
HIGH: LPC SELECTED FOR SYSTEM FLASH  
WEAK INTERNAL PD

1212 change R95 pull-high from +3V to +3V\_DEEP\_SUS



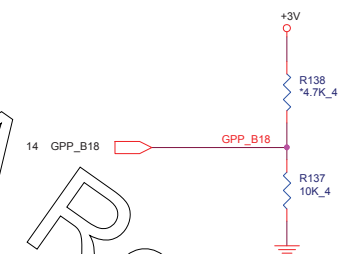
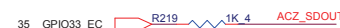
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).  
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



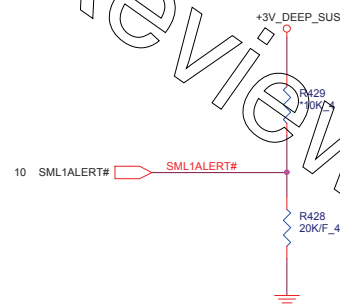
**No Boot:**  
The signal has a weak internal pull-down.  
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.  
Bit 10      Boot BIOS Destination  
0            SPI  
1            LPC



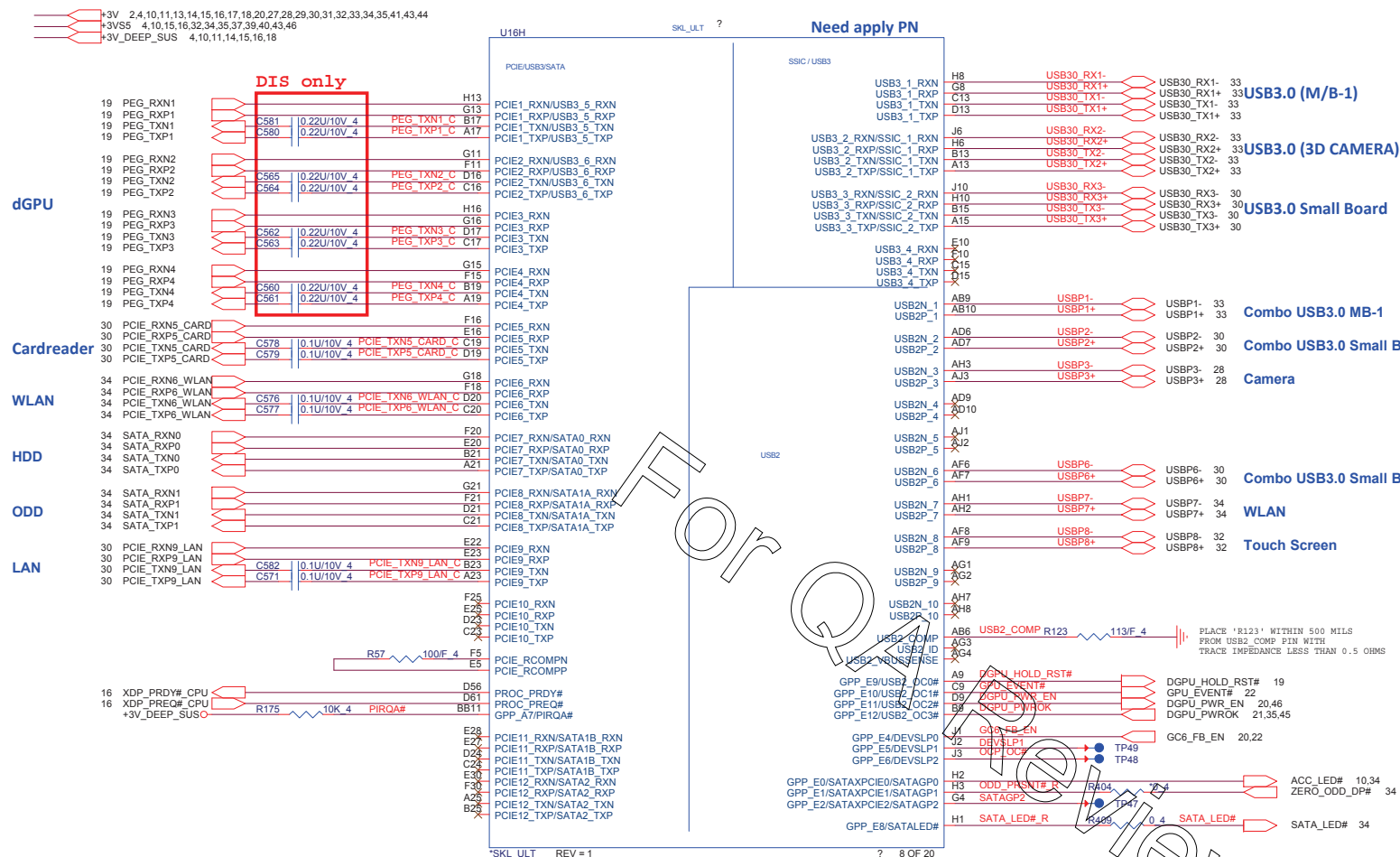
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor.  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable No Reboot mode.  
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature).  
This function is useful when running ITP/XDP.



**No Boot:**  
The signal has a weak internal pull-down.  
0 = LPC is selected for EC.  
1 = eSPI is selected for EC.



### PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	Un-used
Port2	dGPU	Port1	CardReader
Port3	dGPU	Port2	WLAN
Port4	dGPU	Port3	LAN
Port5	CardReader	Port4	VGA
Port6	WLAN	Port5	Un-used
Port7	HDD		
Port8	ODD		
Port9	LAN		
Port10	Un-used		

### USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	NC
PORT-3	Cobime USB3.0 Smaii Board
PORT-4	NC

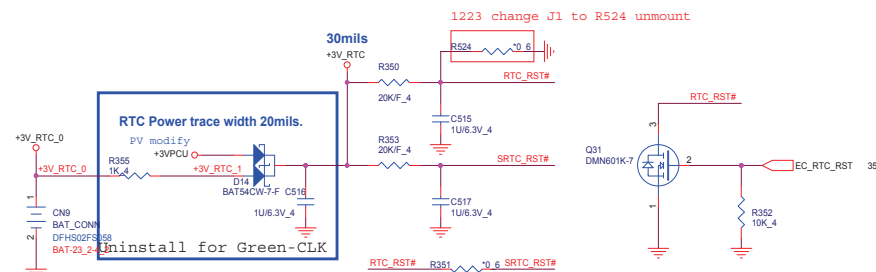
## USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB-1
PORT-2	Cobime USB3.0 Smail Board
PORT-3	Camera
PORT-4	NC
PORT-5	NC
PORT-6	Cobime USB3.0 Smail Board
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

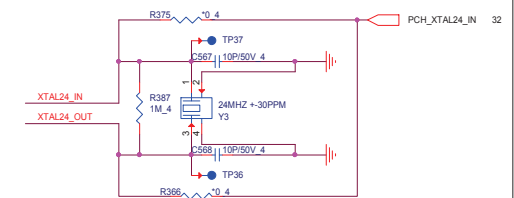


**PROJECT :Y11X-6L**  
Quanta Computer Inc.

Size Custom	Document Number <b>12 -- SKYPAKE 16/20 (PCIE/USB)</b>	Rev 1A
Date: Wednesday, May 06, 2015	Sheet 12 of	49



The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.



0305  
Change C567 and C568 to 10pf



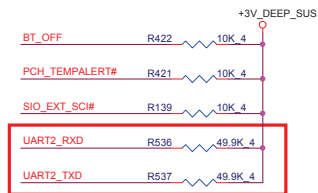
**PROJECT :Y11X-6L**  
Quanta Computer Inc.

Size Custom	Document Number <b>13 -- SKYPAKE 17/20 (CLK)</b>	Rev 1A
Date: Wednesday, May 06, 2015	Sheet	13 of 49



## Skylake (GPIO)

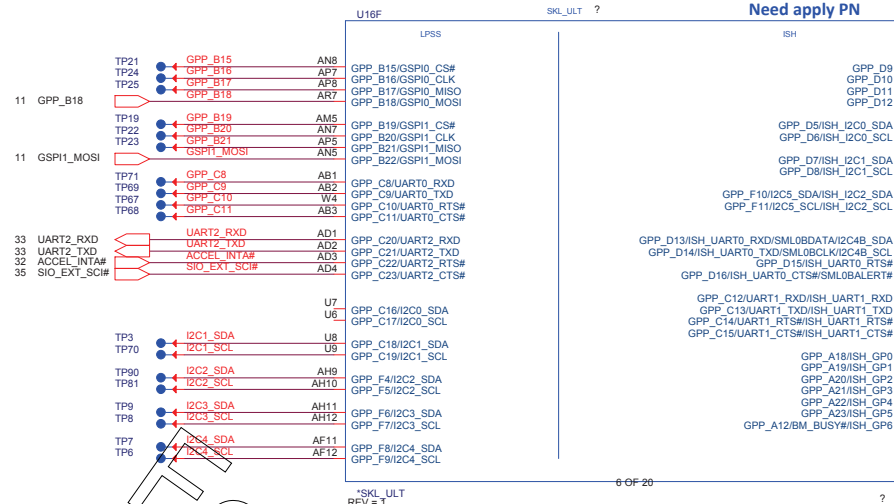
+3V 2,4,10,11,12,13,15,16,17,18,20,27,28,29,30,31,32,33,34,35,41,43,44  
+3V\_DEEP\_SUS 4,10,11,12,15,16,18



1227 Add R536 and R537 for  
UART2 function reserved



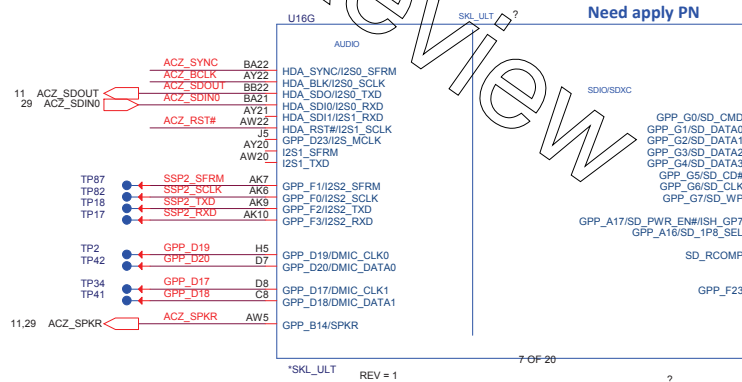
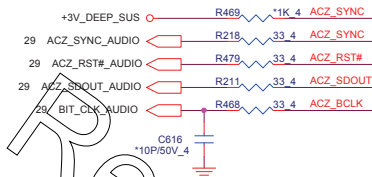
1223 Add R525



0224  
Unmount R547  
0114  
Del TP57, Add R547 with 0ohm

0305  
Del TP73

## HDA Bus(CLG)

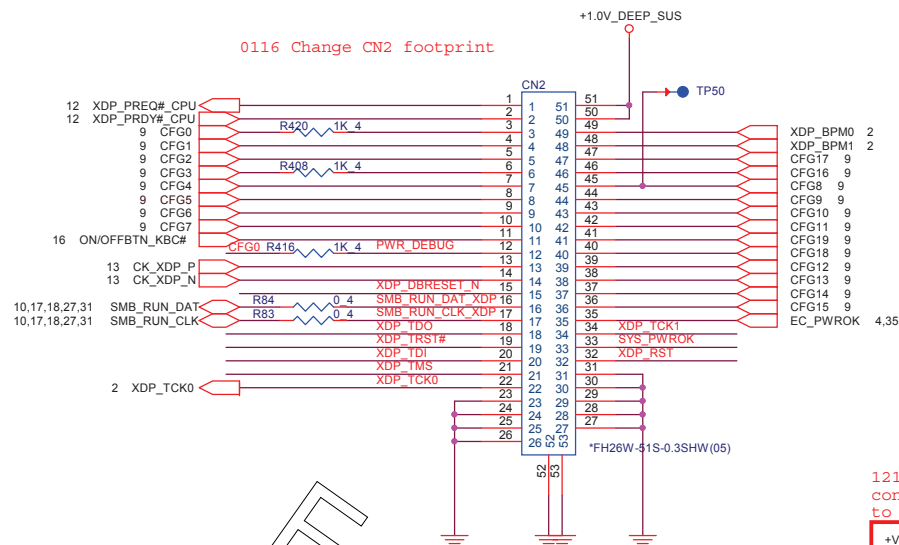


0129  
Del TP110 add GPP\_A16

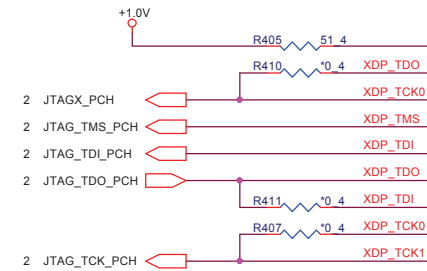
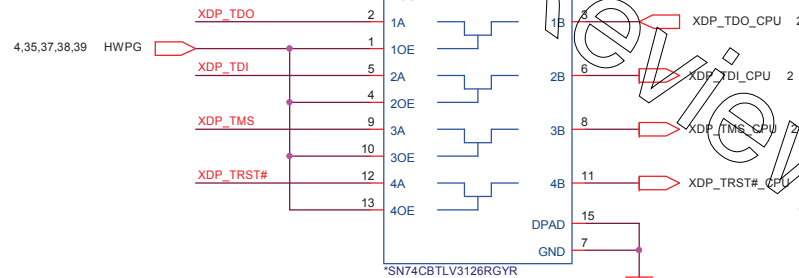
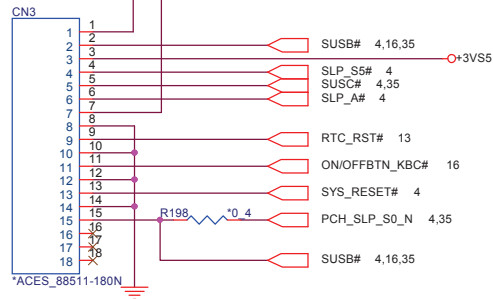
Skylake	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6 ID5	ID4 ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	Reserve (Default = 00)	00 Single Rank (X1B) 01 Dual Rank (X1B) 10 Meso-AMD (X1A) 11 Reserve	00 14" 01 15" 10 17" 11 Reserve	0 : UMA 1 : DIS



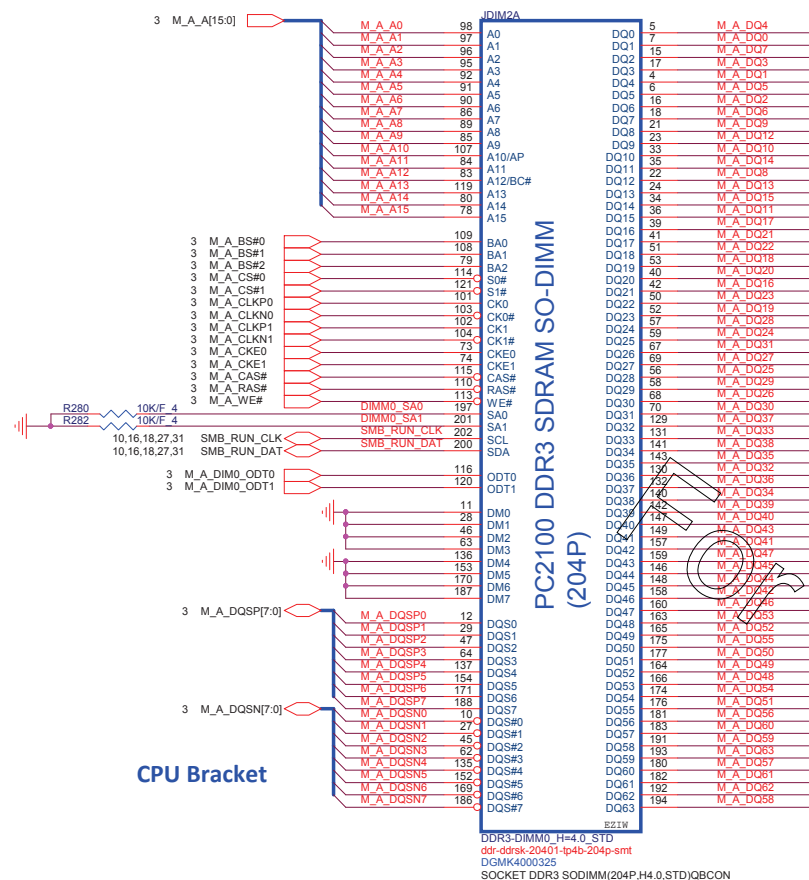
0116 Change CN2 footprint

1218 Change R86  
connection from +1.0V  
to +VCCIO

APS

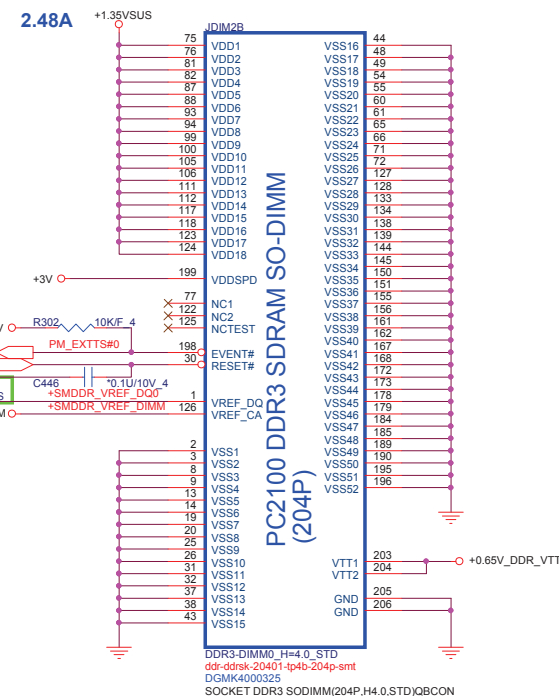


**PROJECT :Y11X-6L**  
**Quanta Computer Inc.**

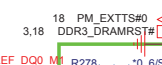


CPU Bracket

M\_A\_DQ[63:0] 3

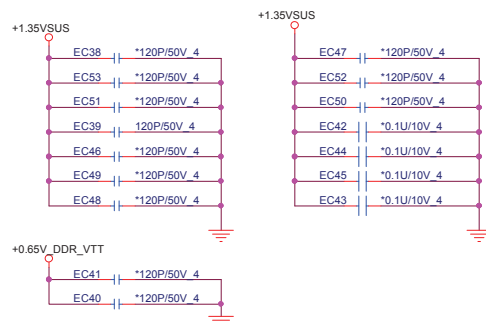


PV modify to short pad



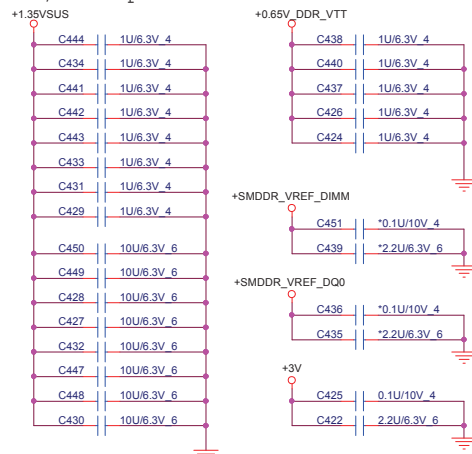
QA Review

## For EMI RESERVE

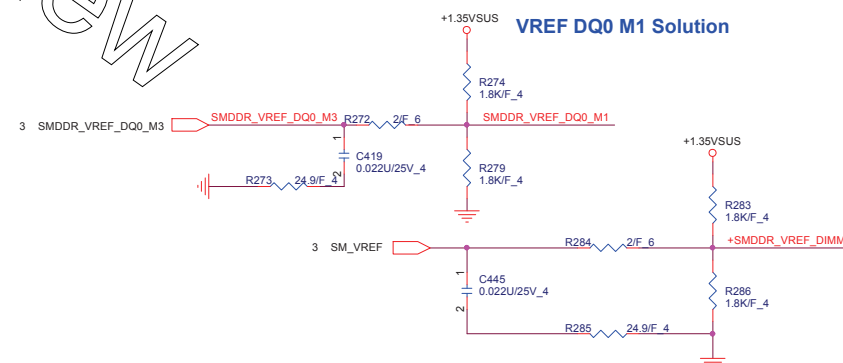


## Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector



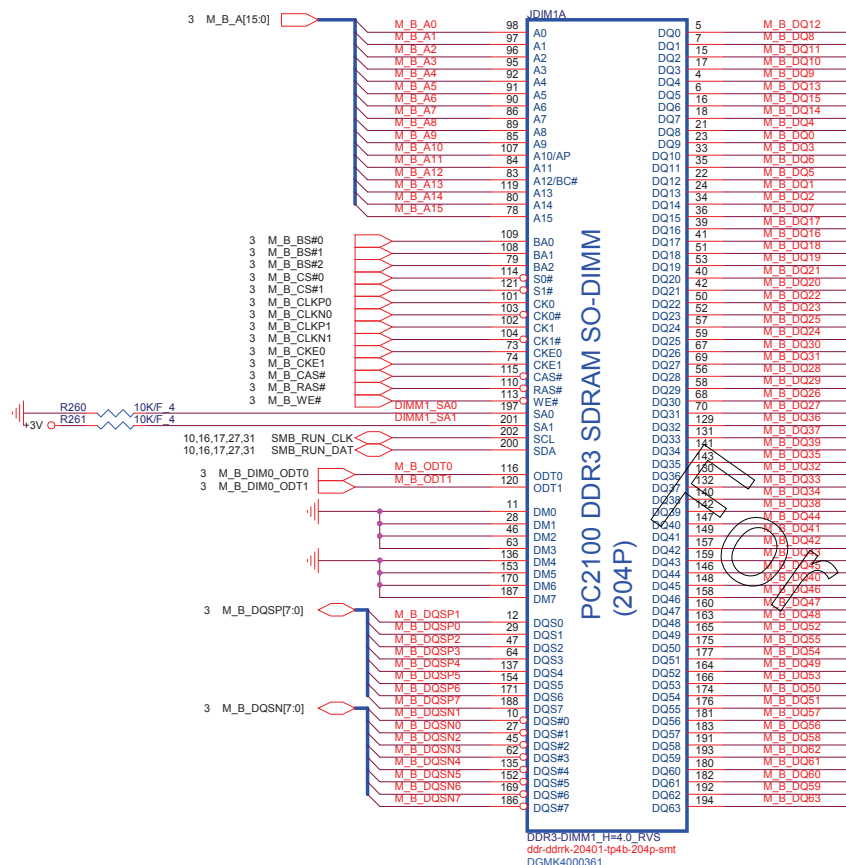
## VREF DQ0 M1 Solution



**PROJECT :Y11X-6L**  
**Quanta Computer Inc.**

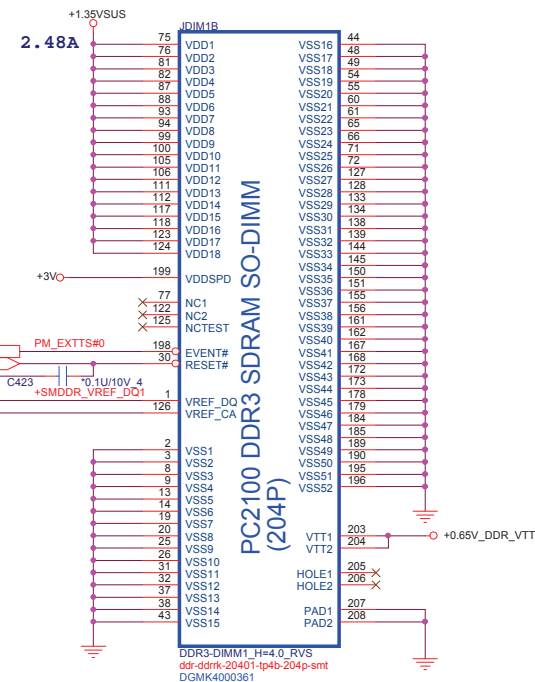
Size	Document Number	Rev
Custom	17 - DDR3 DIMM0-STD(4.0H)	1A
Date:	Wednesday, May 06, 2015	Sheet 17 of 49

M\_B\_DQ[63:0] 3

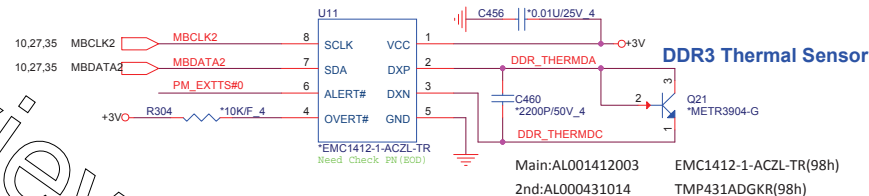


PV modify to short pad

SMDR\_VREF\_DQ1\_M1

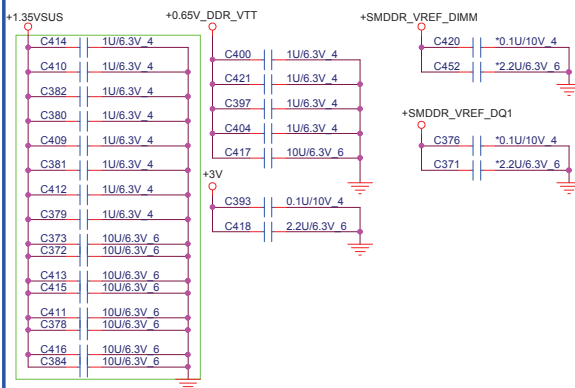


Local Thermal Sensor 1223 R304, U11, C460, C456, Q21 mount

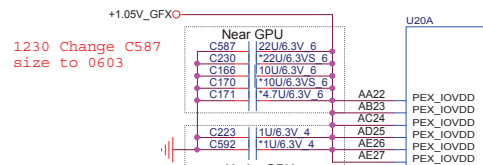


Place these Caps near So-Dimm1.

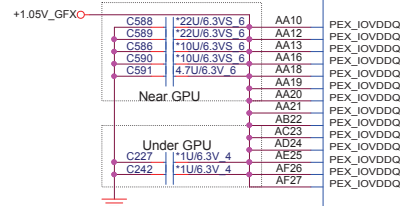
1uF/10uF 4pcs on each side of connector



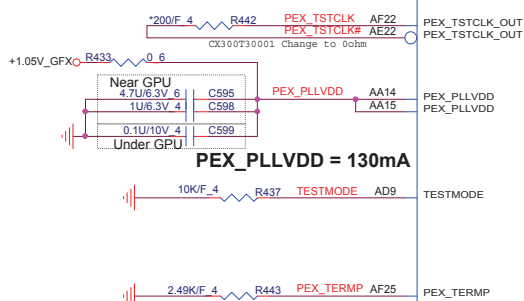
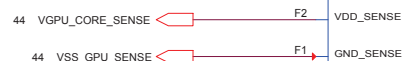
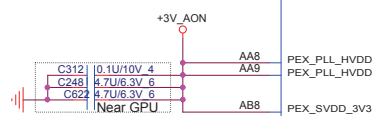




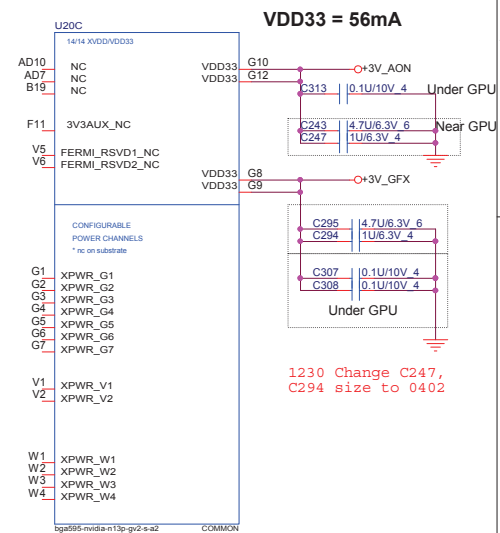
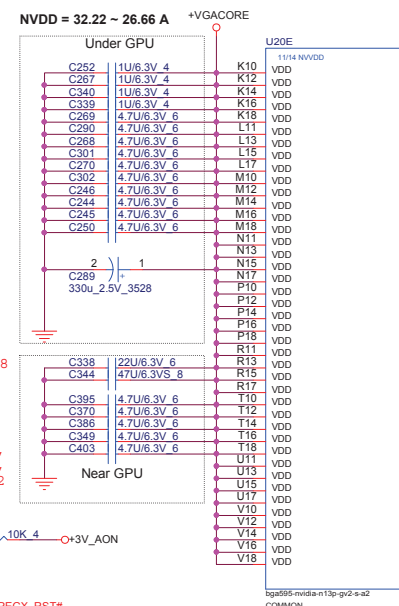
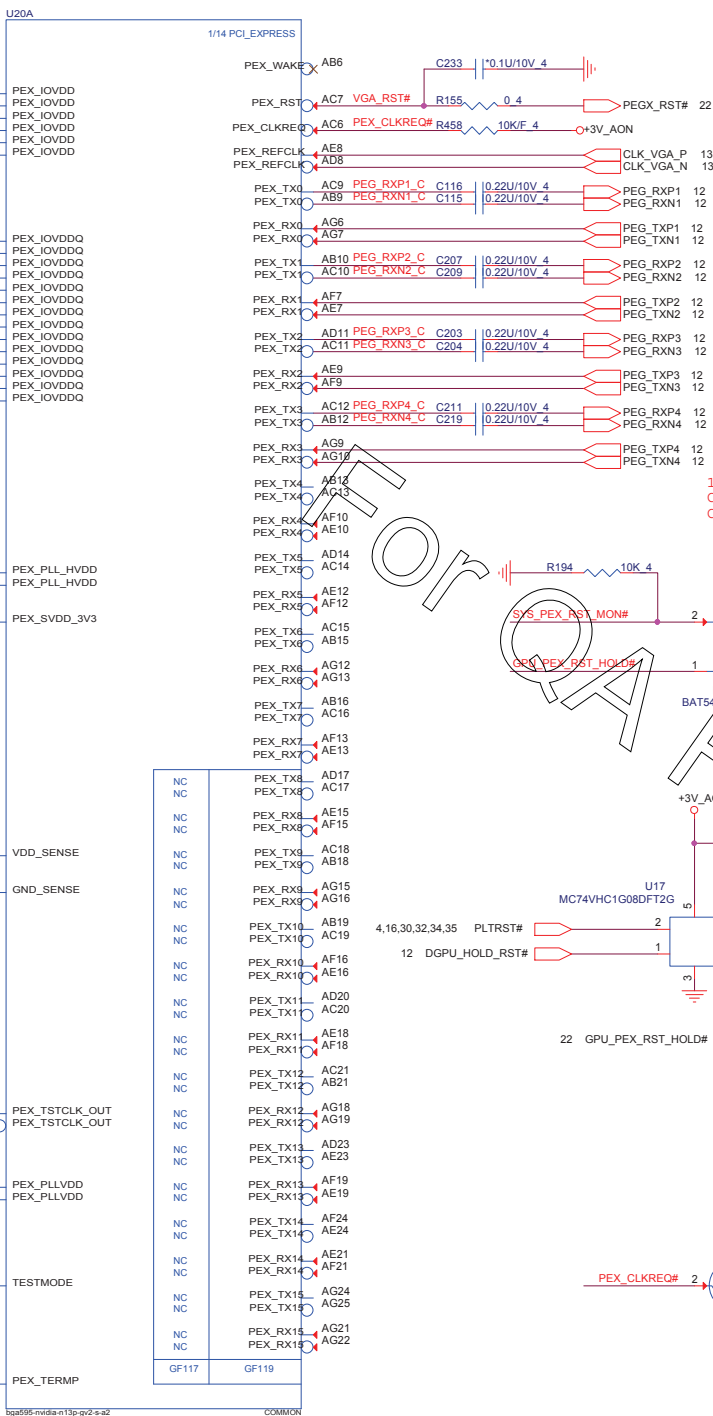
PEX\_IOVDD + PEX\_IOVDDQ = 1.042A



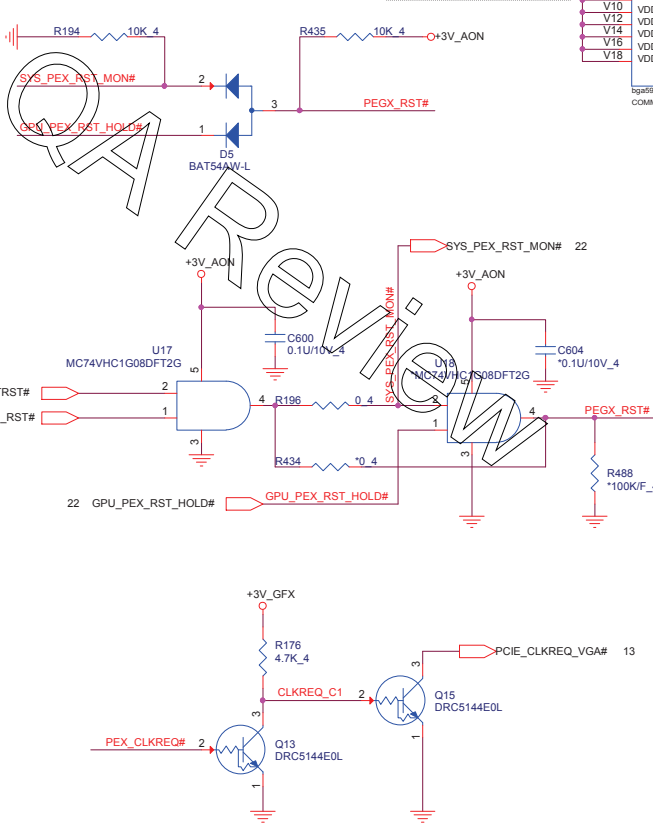
PEX\_PLL\_HVDD + PEX\_SVDD\_3V3 = 143mA



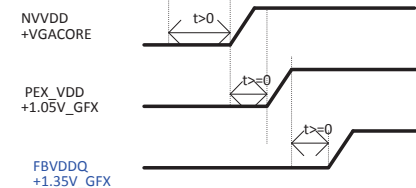
PEX\_PLLVDD = 130mA



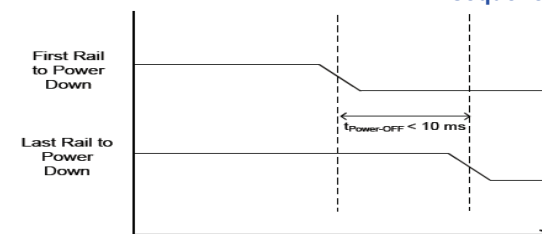
1230 Change C247, C294 size to 0402

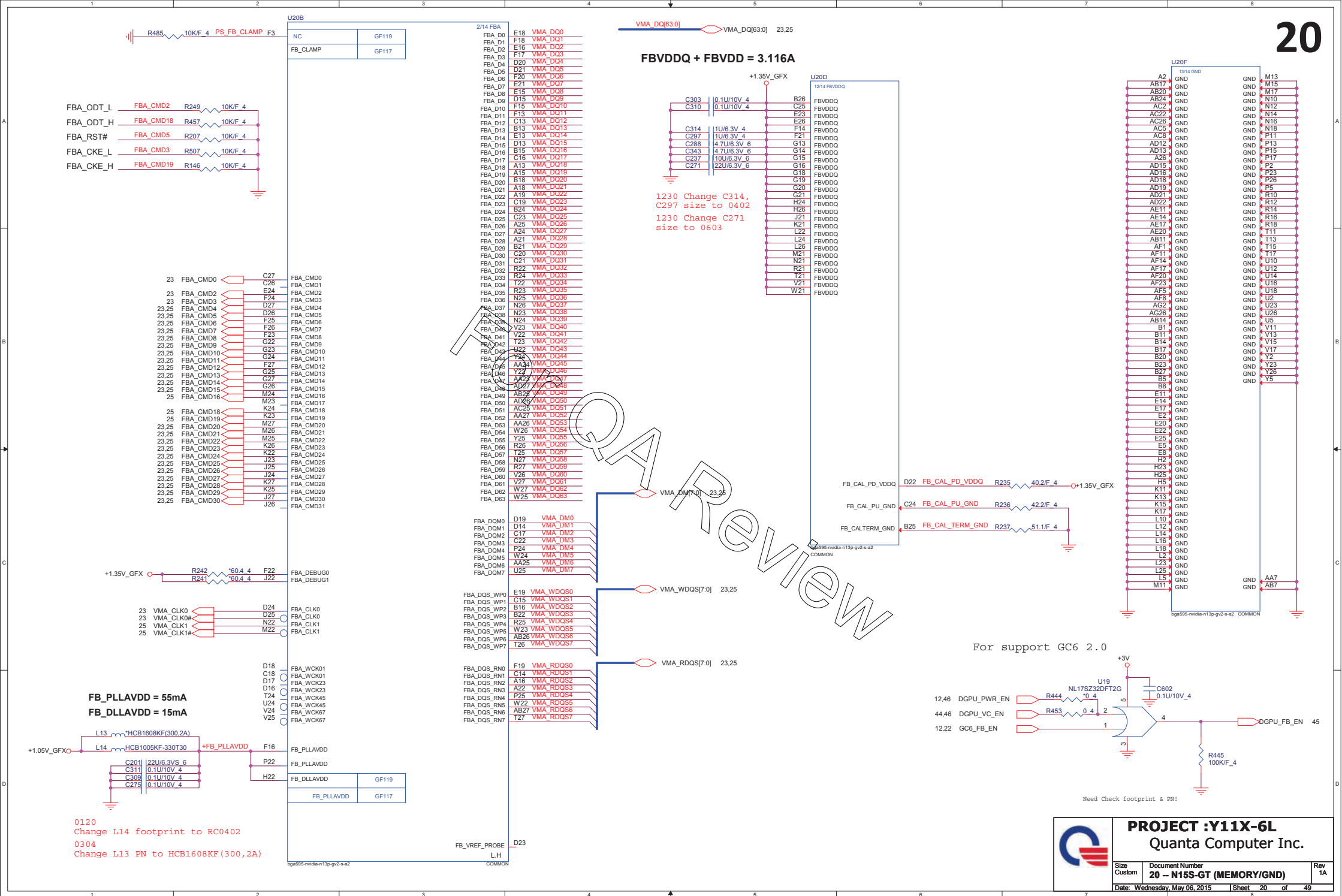


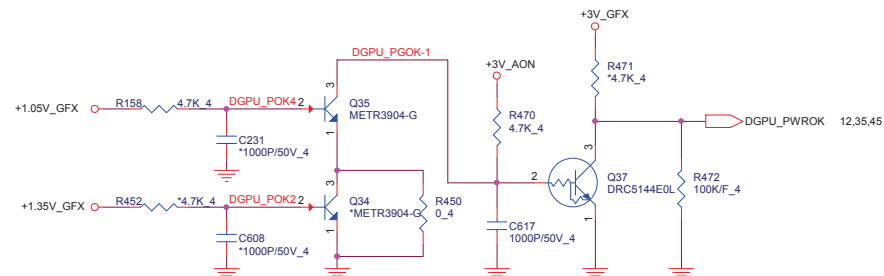
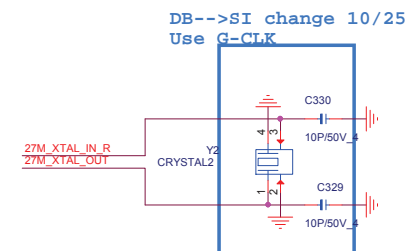
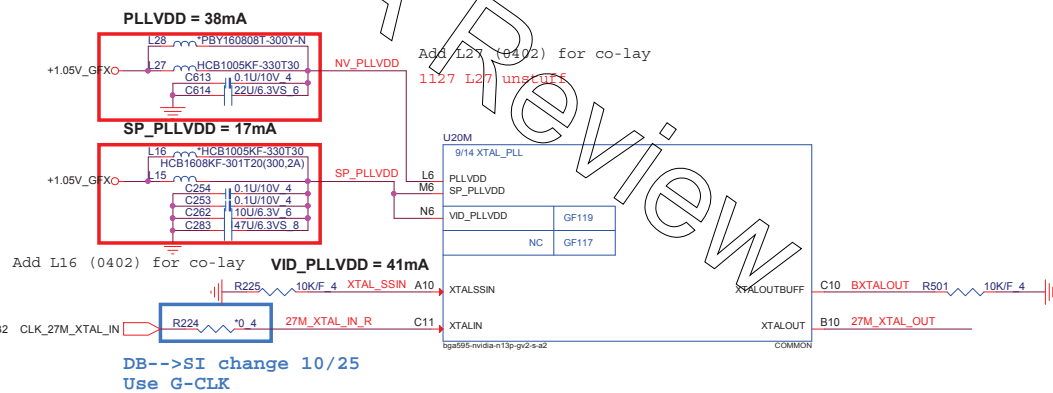
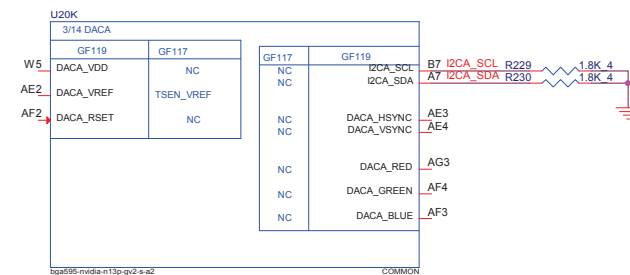
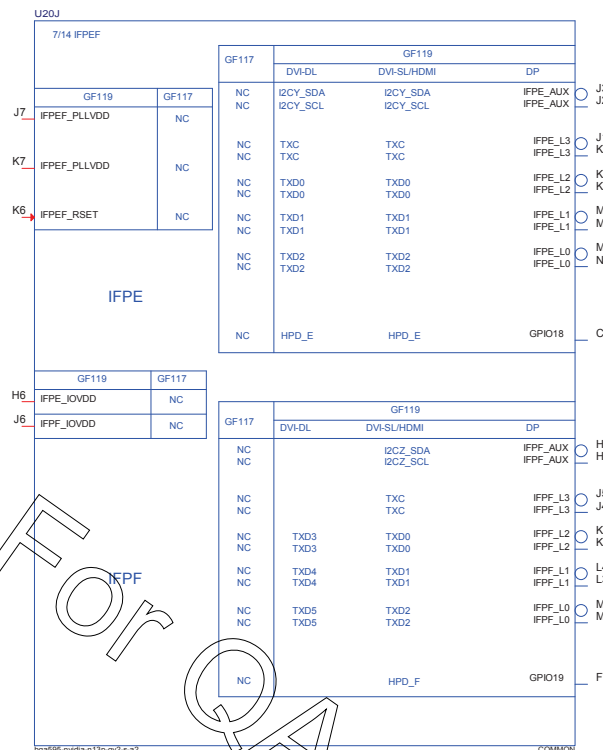
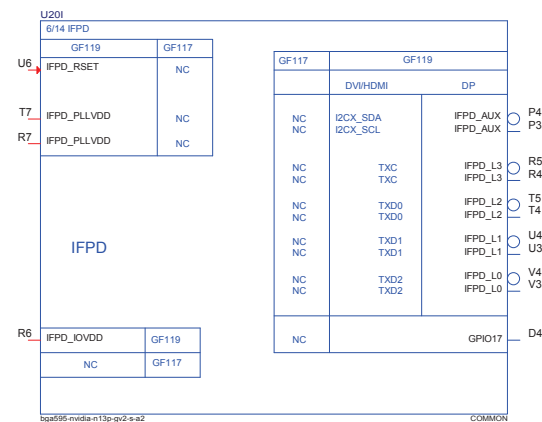
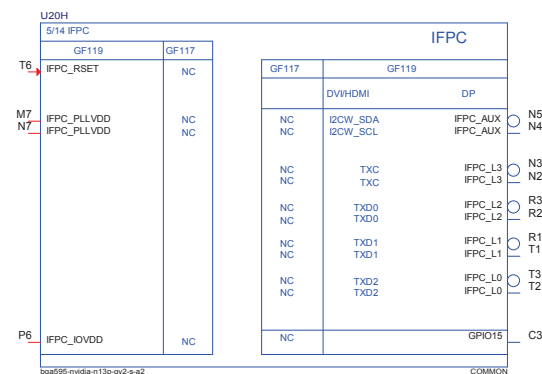
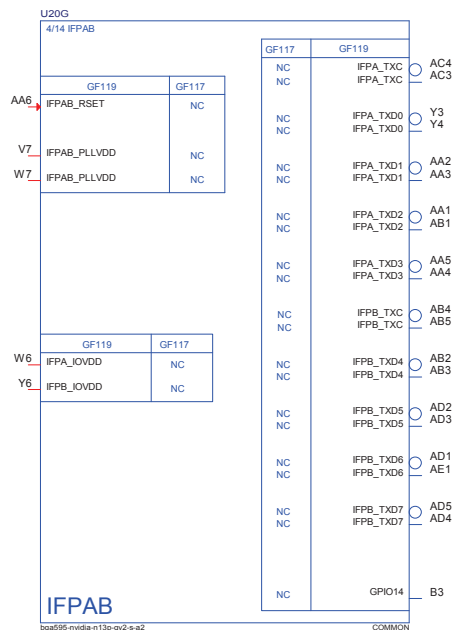
Power up sequence



Power down sequence







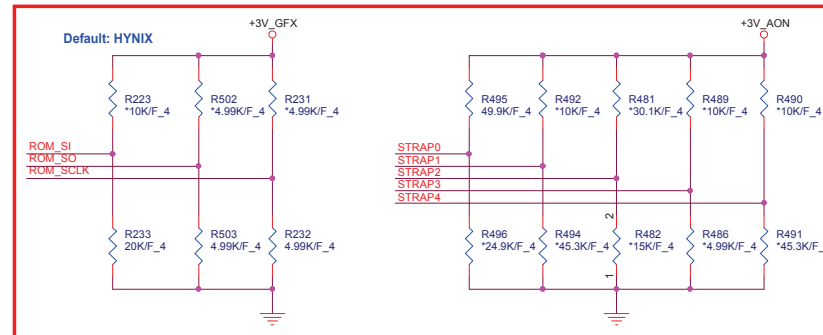
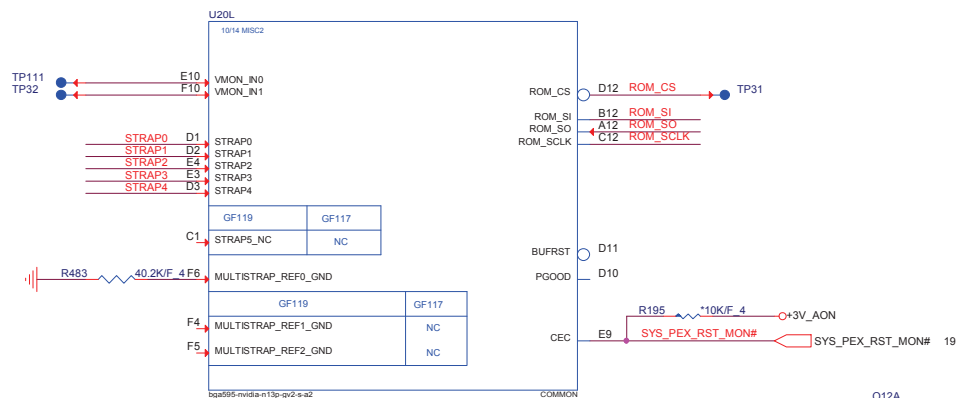
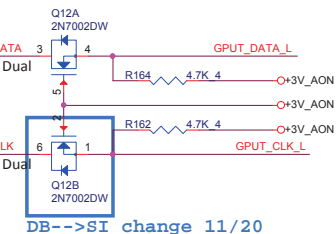
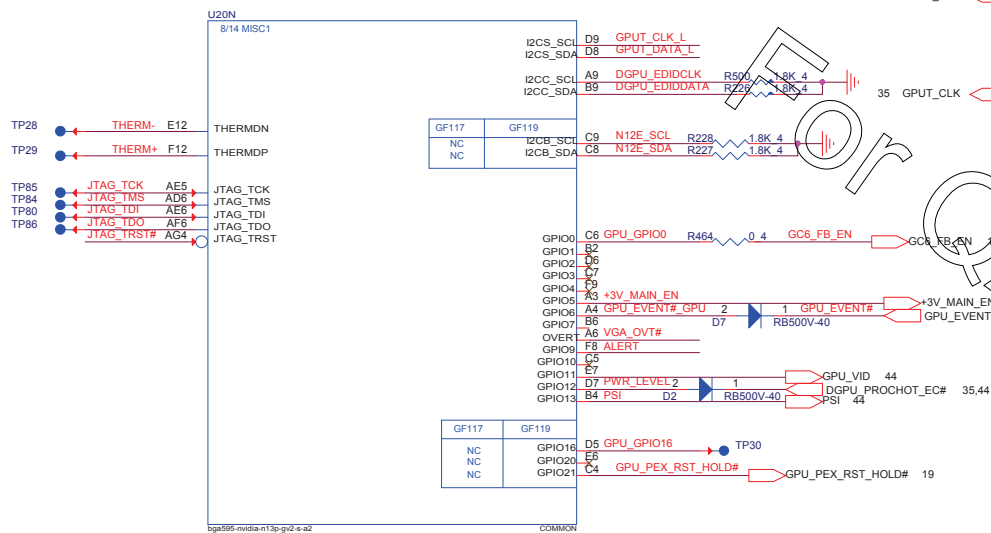


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



VRAM Configuration Table ROM\_SI S F

RAMCFG (3:0)	DESCRIPTION	Vendor	Vendor P/N	Strapping	TOP B/S	QBC
0000	DDR3L 256Mx16, 64bit, 4Gb, 900MHz	HYNIX	H5TC4G63CFR-N0C	0x2	AKD5PZDTW01	AKD5PZDTW02
0010	DDR3L 256Mx16, 64bit, 4Gb, 900MHz	Micron	MT41J256M16HA-093G:E	0x4	AKD5PZSTL00	AKD5PZSTL01
0100	DDR3L 256Mx16, 64bit, 4Gb, 900MHz	SAMSUNG	K4W4G1646E-BC1A	0x1	AKD5PGDT500	AKD5PGDT501
0001	DDR3L 256Mx16, 64bit, 4Gb, 900MHz					

## GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

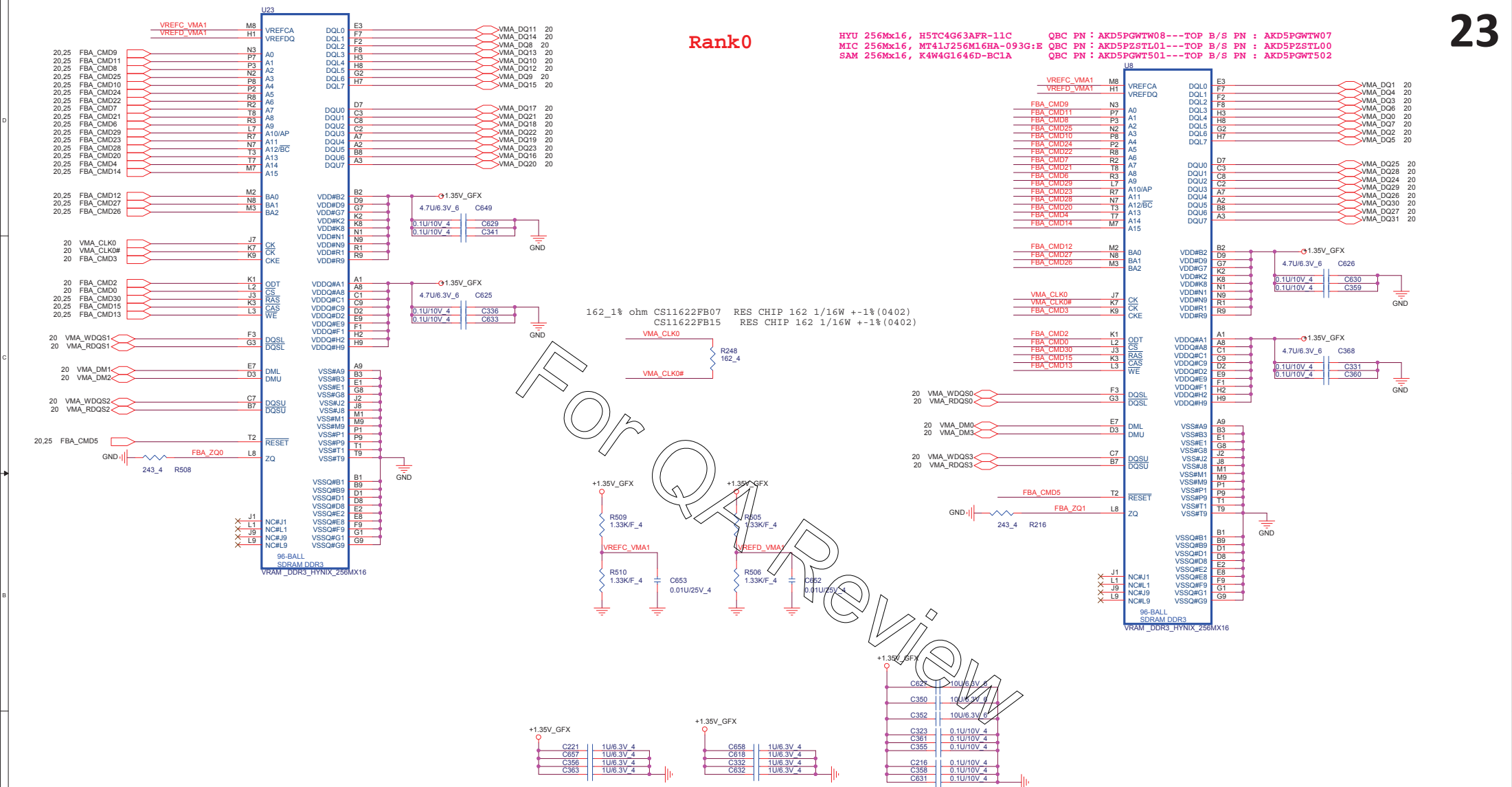


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**Quanta Computer Inc.**

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Rank0

HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07  
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00  
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502



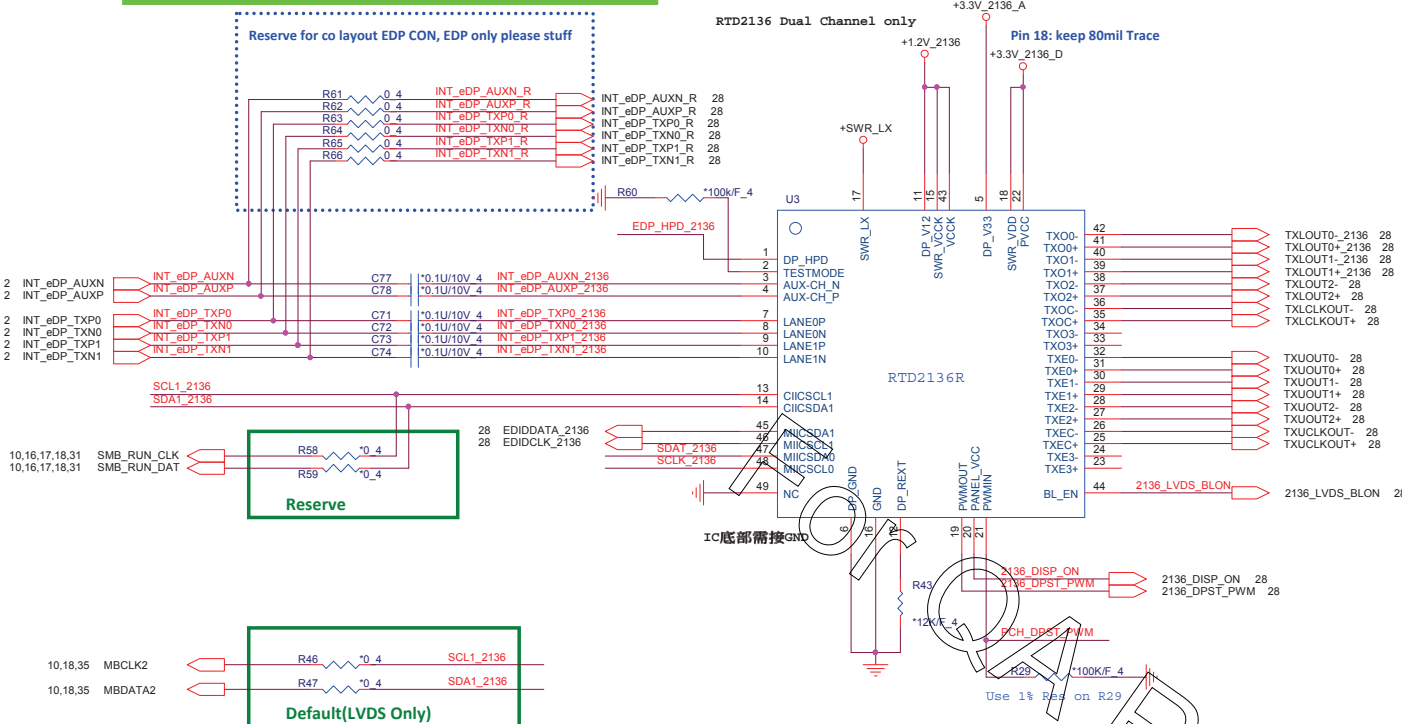
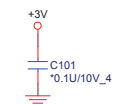
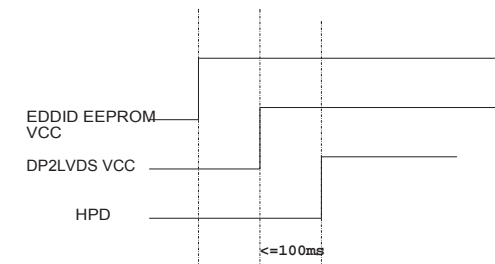


For QA Review

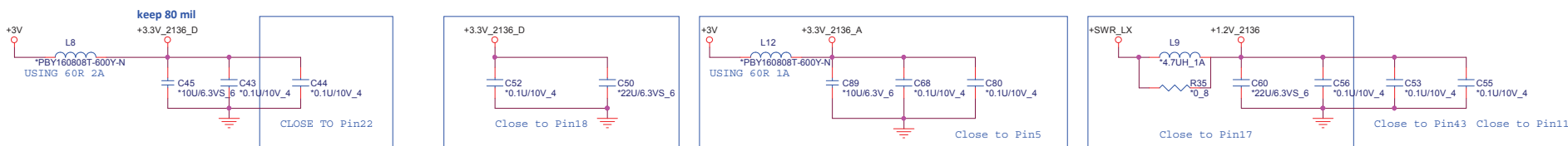


For QA Review

## 27

[illegible]

L9: need use CV-4709MN00 for Vendor suggestion



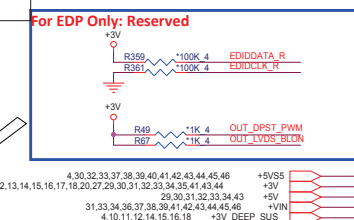
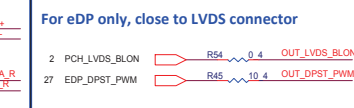
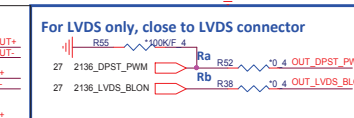
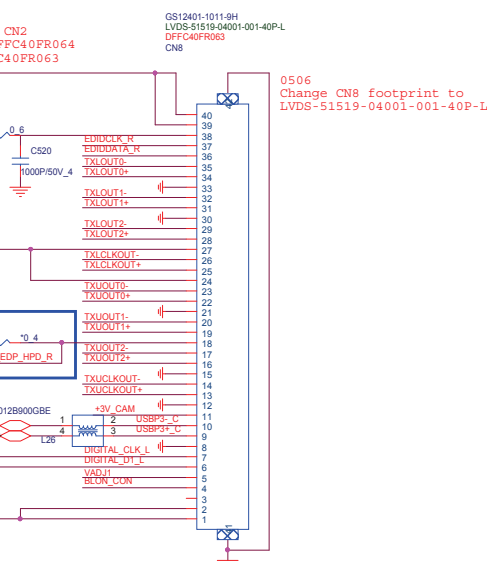
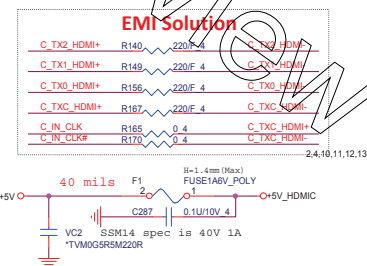
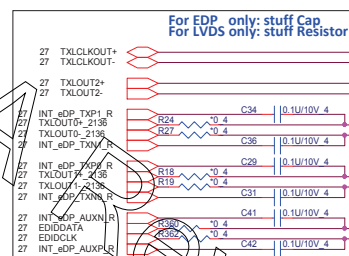
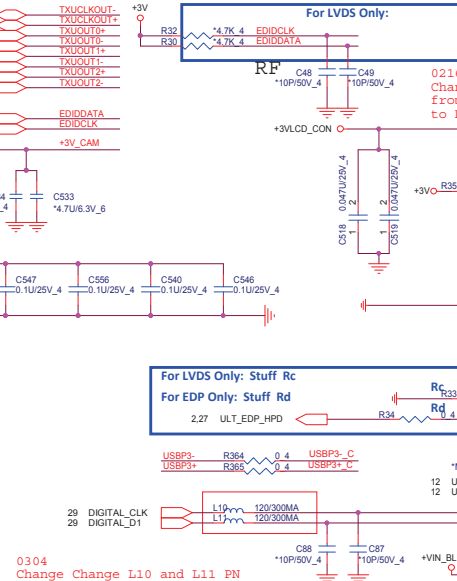
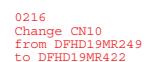
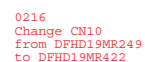
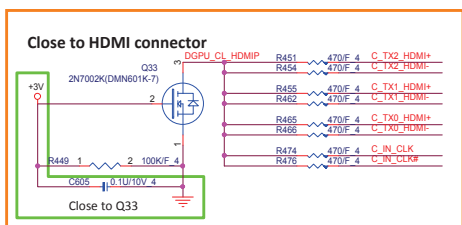
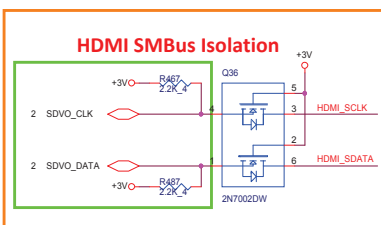
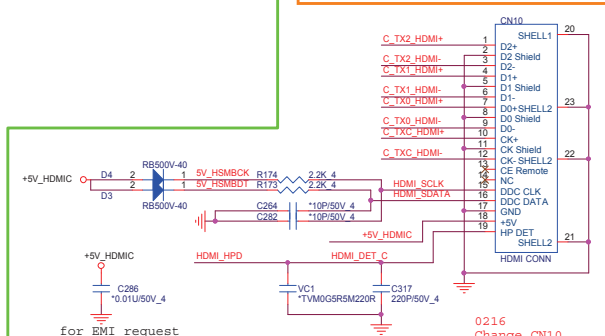
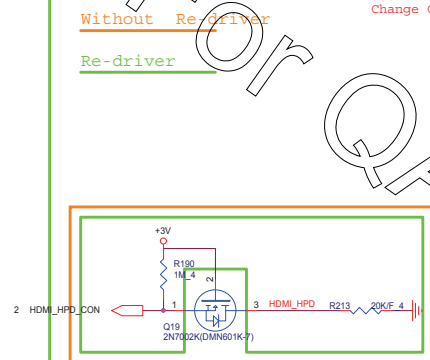
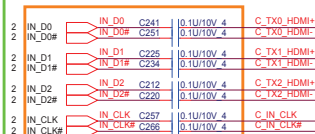
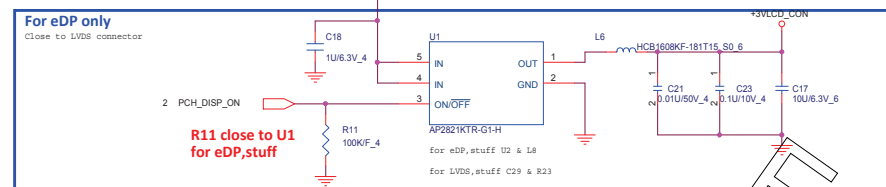
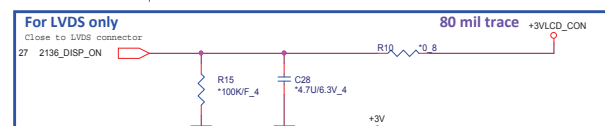
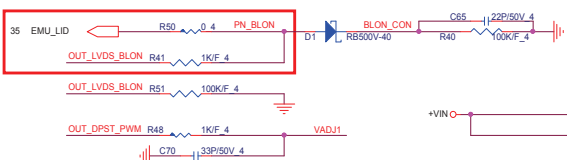
SWR MODE	LDO MODE
Stuff L9	Stuff R35



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Quanta Computer Inc.

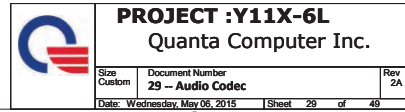
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## LID Switch



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Quanta Computer Inc.

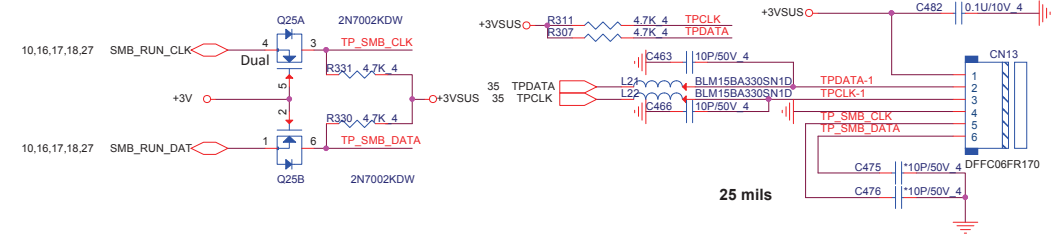






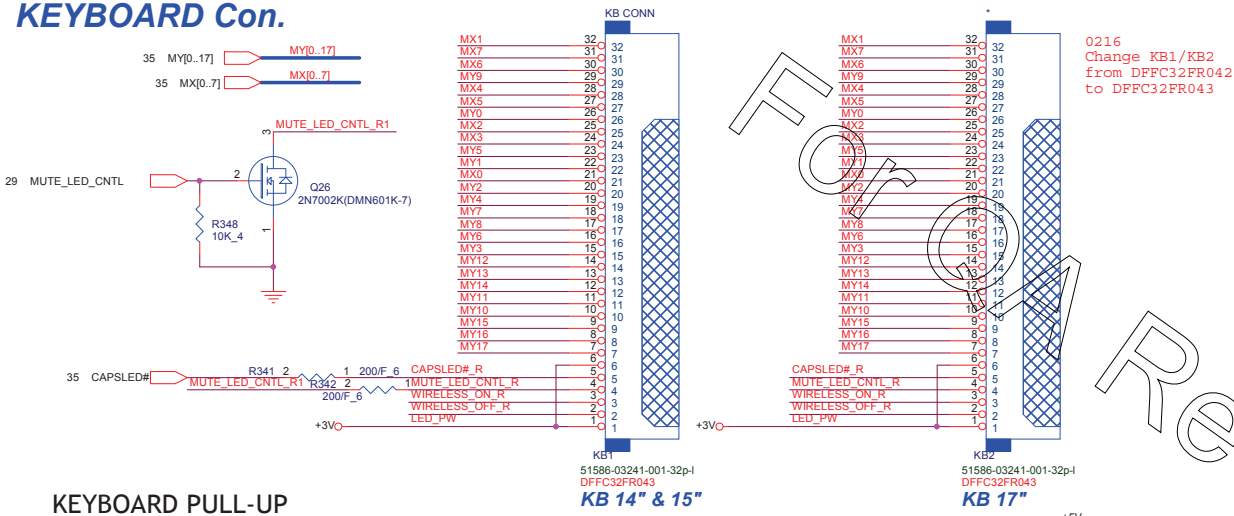
## Touch Pad Connector

31



0216  
Change CN13  
from DFFC06FR162  
to DFFC06FR170

## KEYBOARD Con.

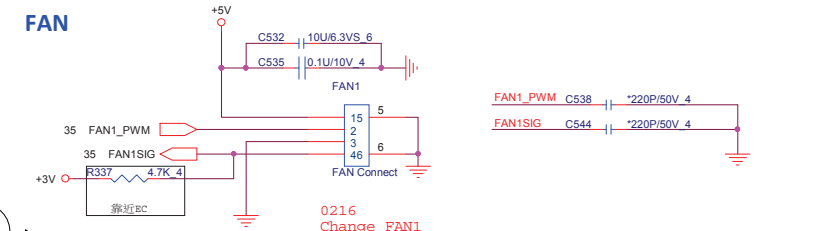


0216  
Change KB1/KB2  
from DFFC32FR042  
to DFFC32FR043

## KEYBOARD PULL-UP



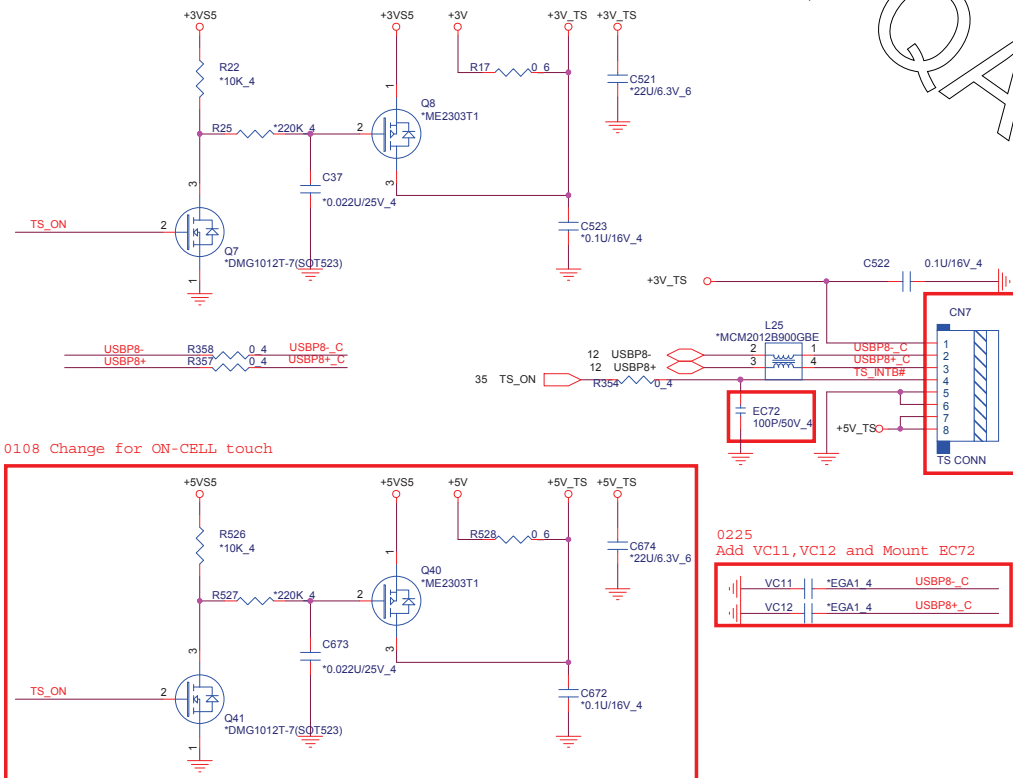
## FAN



0216  
Change FAN1  
from DFHD04MS185  
to DFHD04MR296

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Quanta Computer Inc.		
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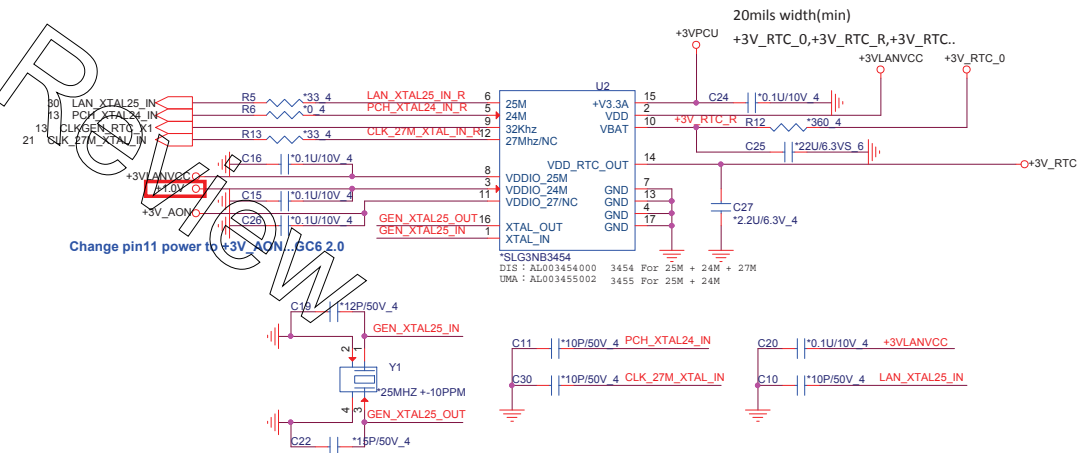
(default)



32

[illegible]

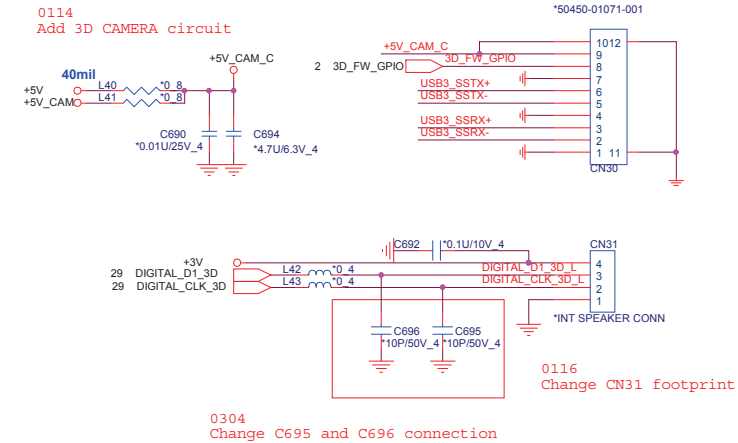
## Green CLK Circuitry



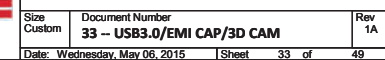
**PROJECT :Y11X-6L**  
Quanta Computer Inc.

Size Custom	Document Number <b>32 -- TPM/G-Sensor/G-CLK/TS/FP</b>	Rev 1A
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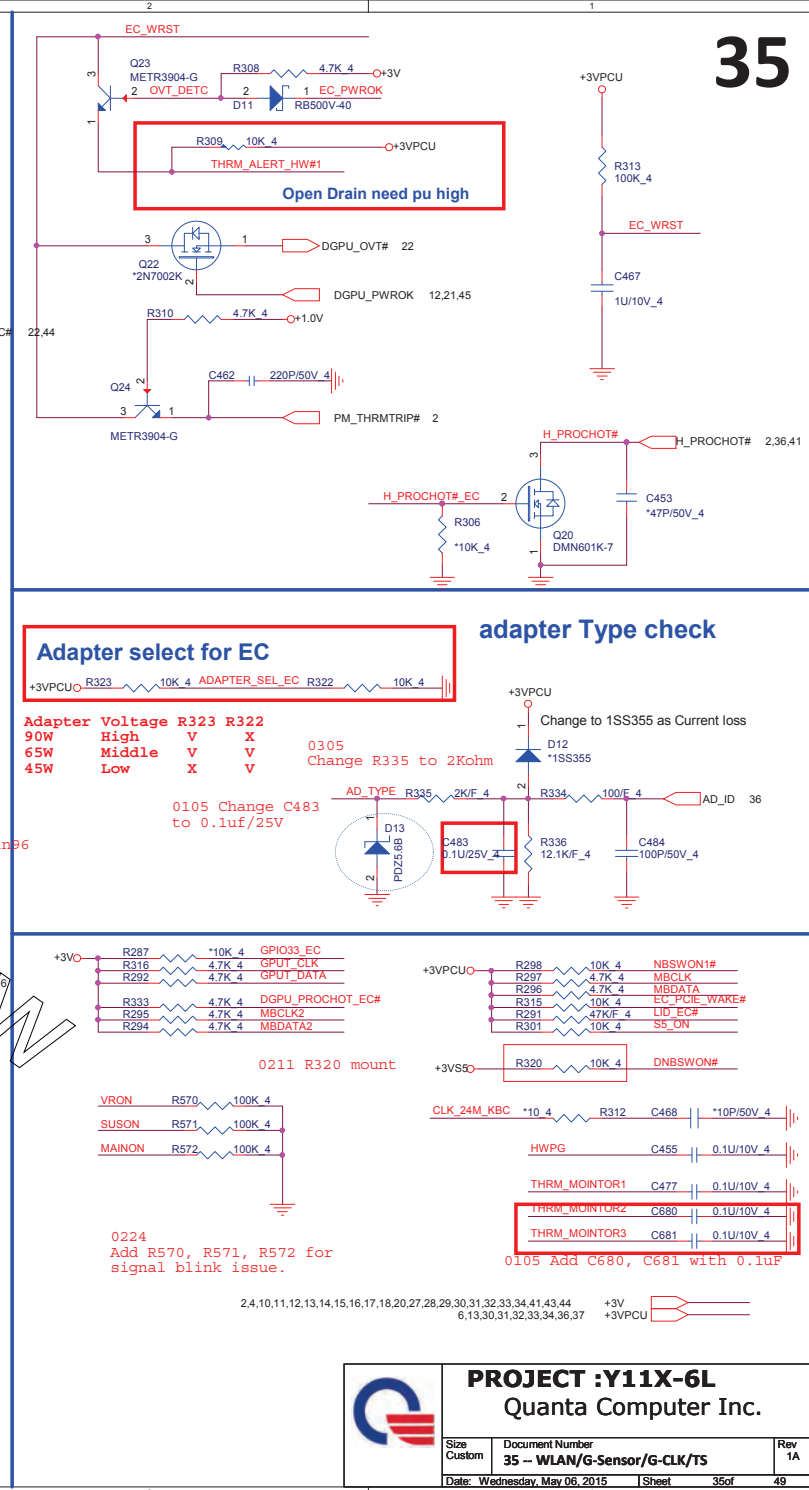


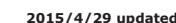
## SI Unmount USB3.0 re-driver for 3D CAMERA

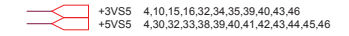






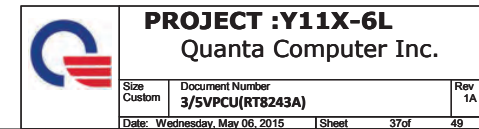


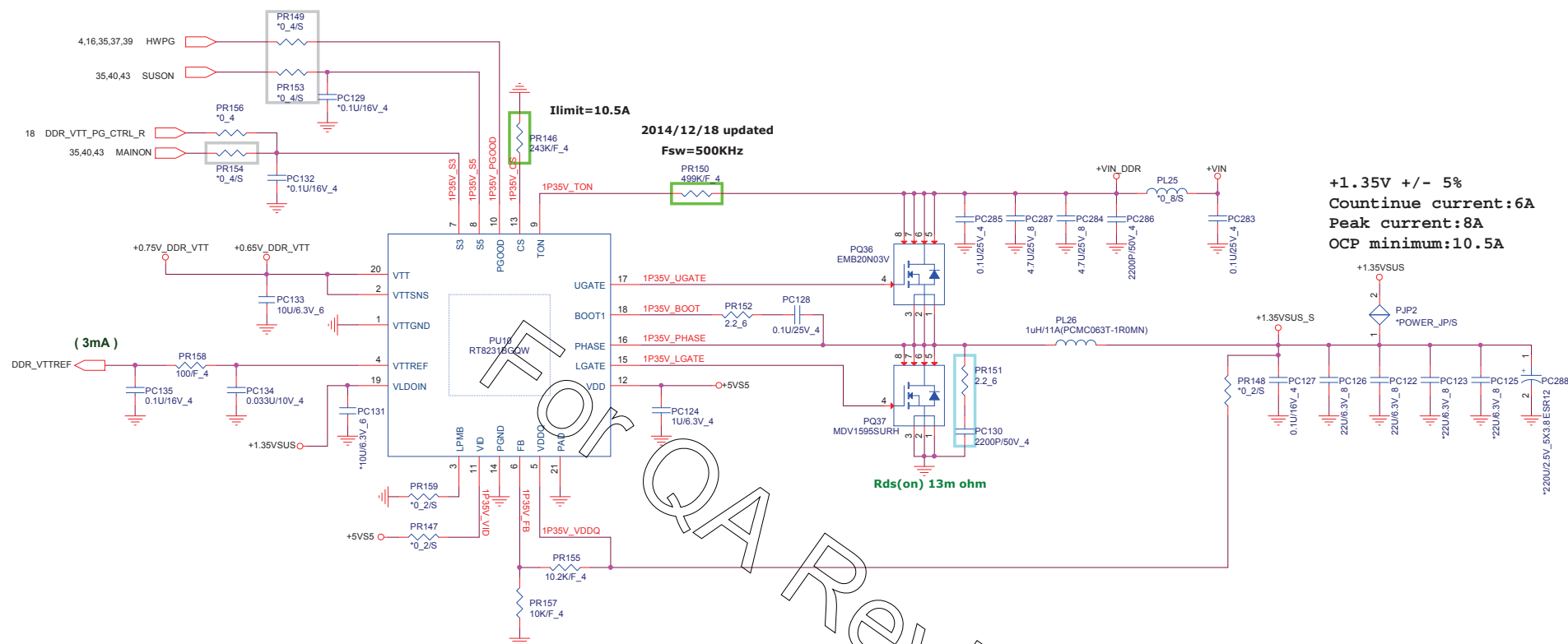


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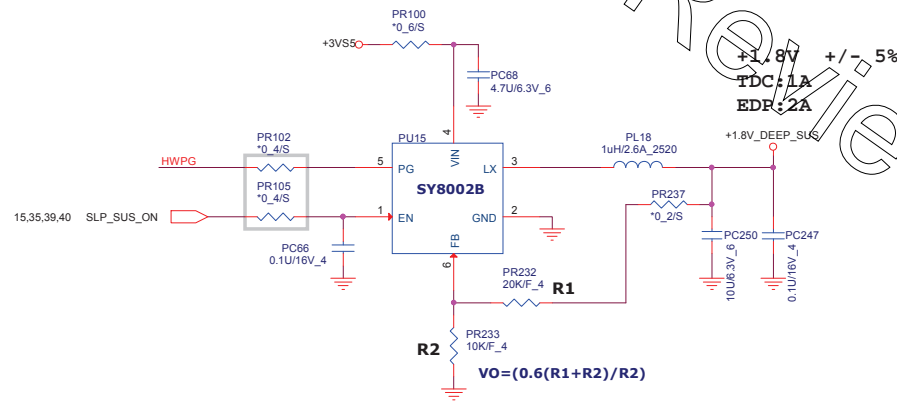
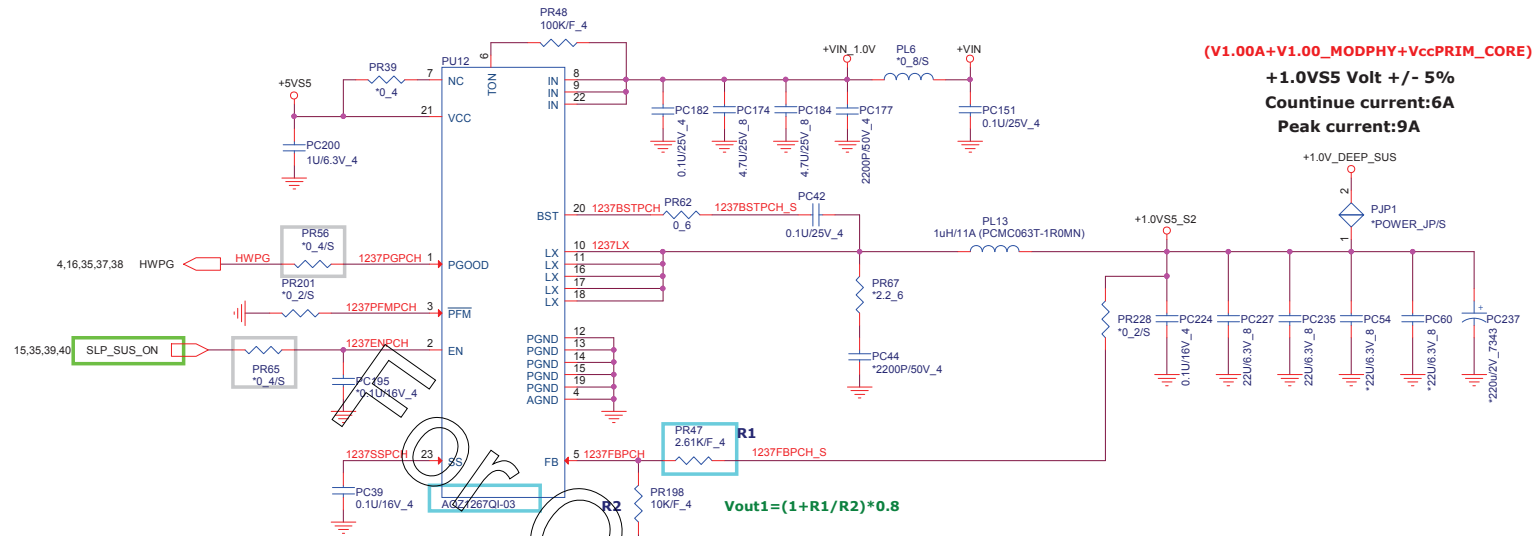
USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff






**Do Not add test pad on VCC & LDO pin**

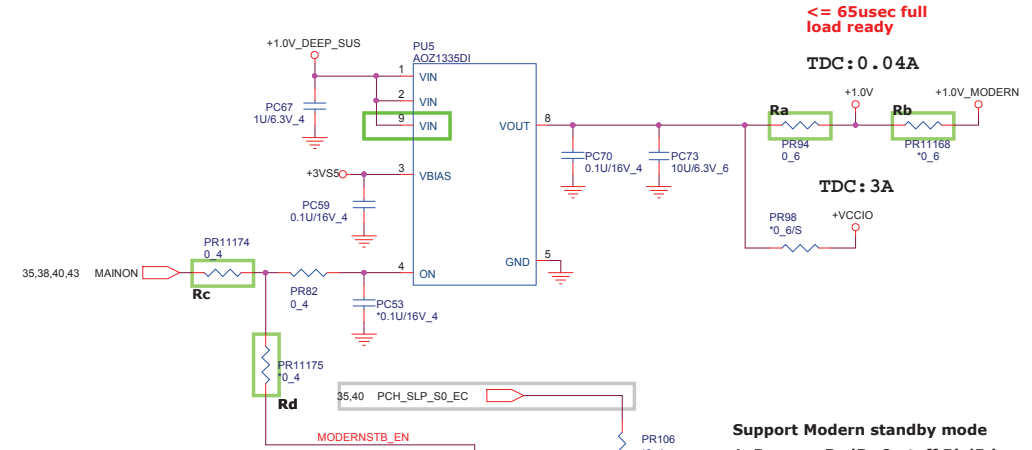
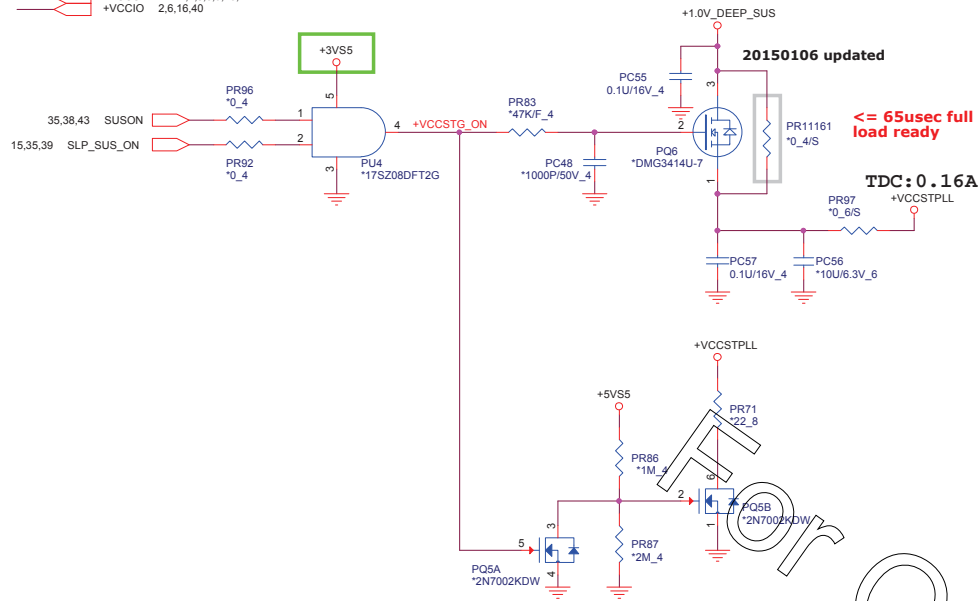




+VIN 28,31,33,34,36,37,38,41,42,43,44,45,46  
 +5VS5 4,30,32,33,37,38,40,41,42,43,44,45,46  
 +3VS5 4,10,15,16,32,34,35,37,40,43,46  
 +1.8V\_DEEP\_SUS 9,15  
 +1.0V\_DEEP\_SUS 9,13,15,16,40



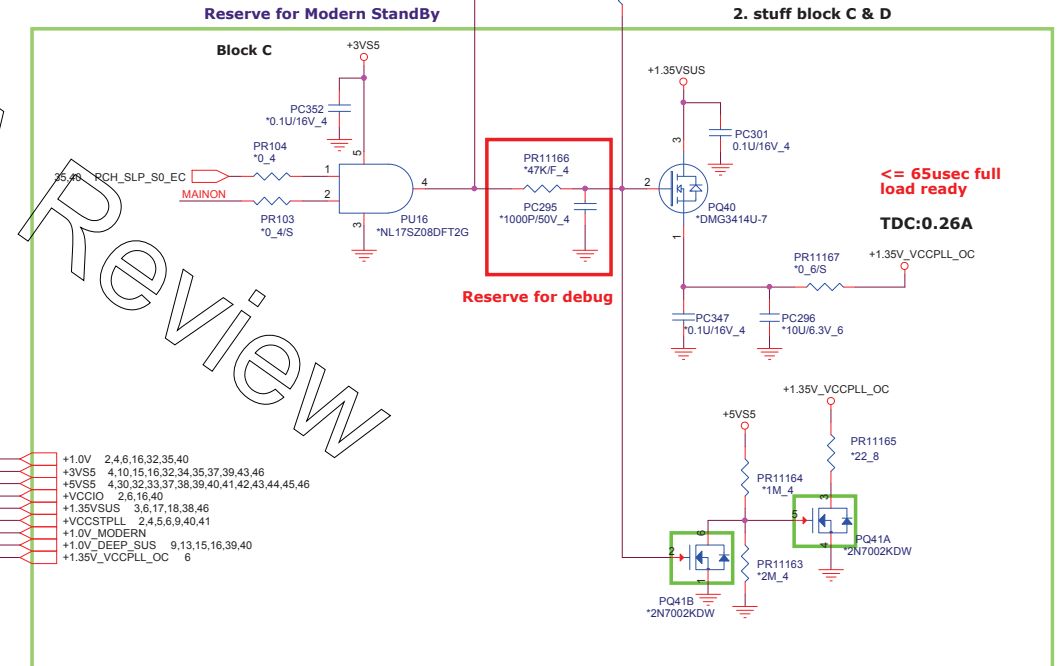
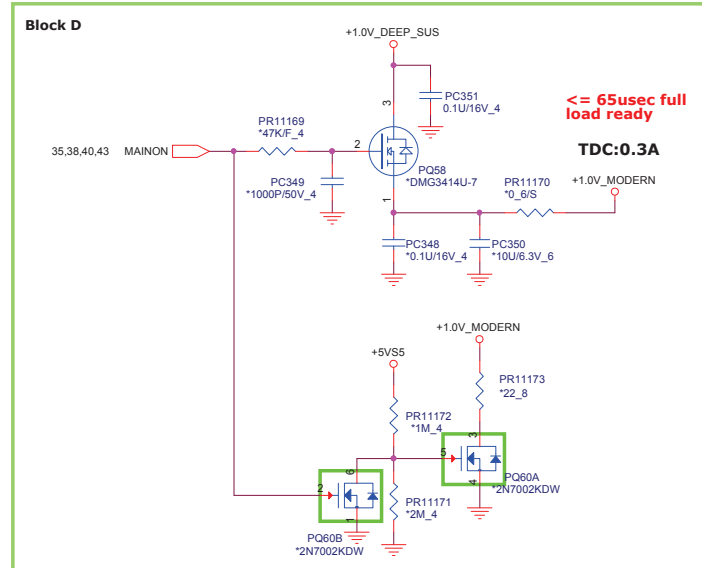
 +1.0V\_DEEP\_SUS 9,13,15,16,39,40  
 +1.0V 2,4,6,16,32,35,40  
 +5VS5 4,30,32,33,37,38,39,40,41,42,43,44,45,46  
 +VCCSTPLL 2,4,5,6,9,40,41  
 +VCCIO 2,6,16,40



**Support Modern standby mode**

- 1. Remove Ra/Rc & stuff Rb/Rd**
- 2. stuff block C & D**

### Reserve for Modern StandBy



Reserve for debug

**<= 65usec full  
load ready**

**TDC:0.26A**

```

+1.0V      2,4,6,16,32,35,40
+3VSS      4,10,15,16,32,34,35,37,39,43,46
+5VSS      4,30,32,33,37,38,39,40,41,42,43,44,45,46
+VCCIO     2,6,16,40
+1.35VSUS  3,6,17,18,38,46
+VCCSTPLL  2,4,5,6,9,40,41
+1.0V_MODERN
+1.0V_DEEP_SUS  9,13,15,16,39,40
+1.35V_VCCPLL_OC  6

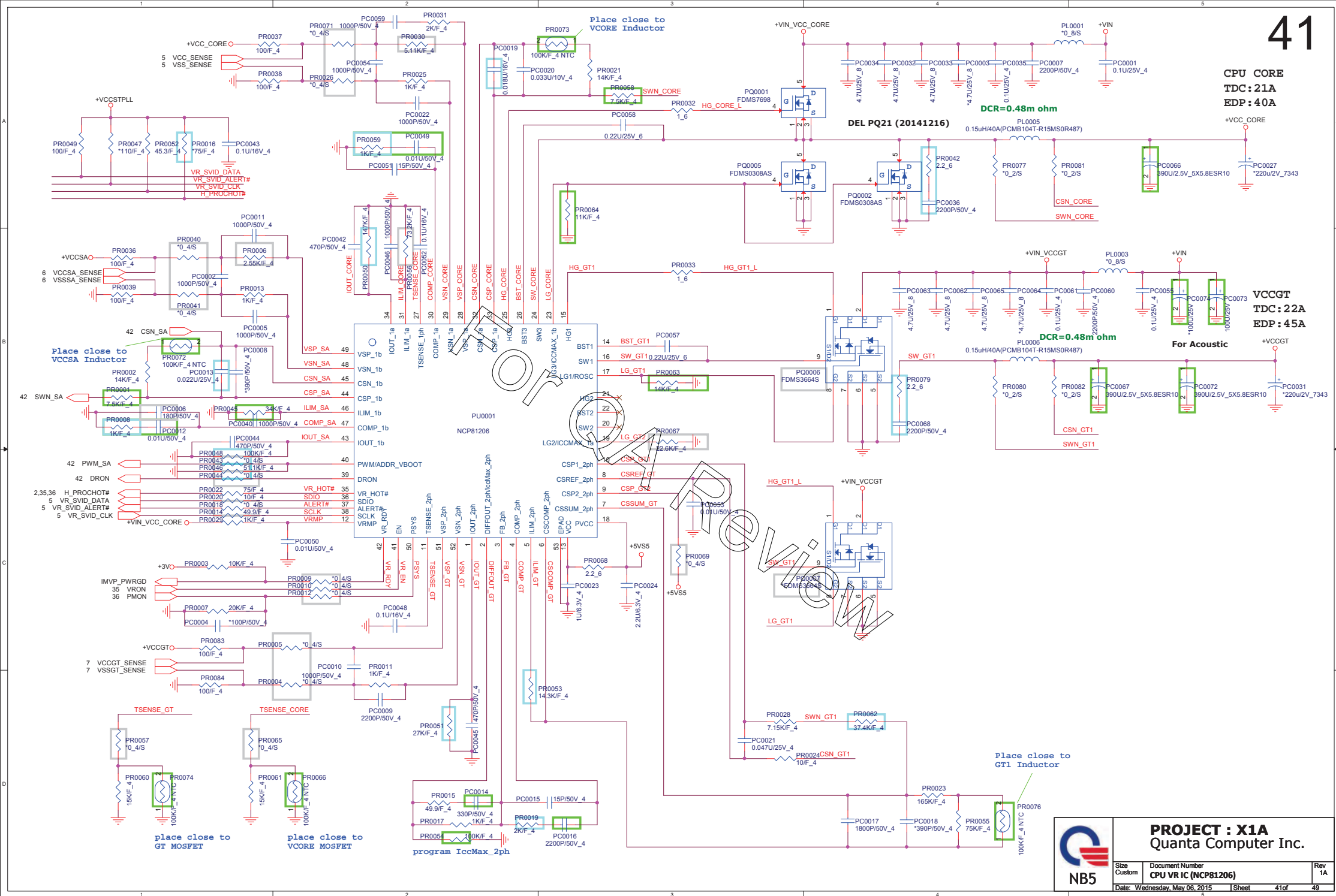
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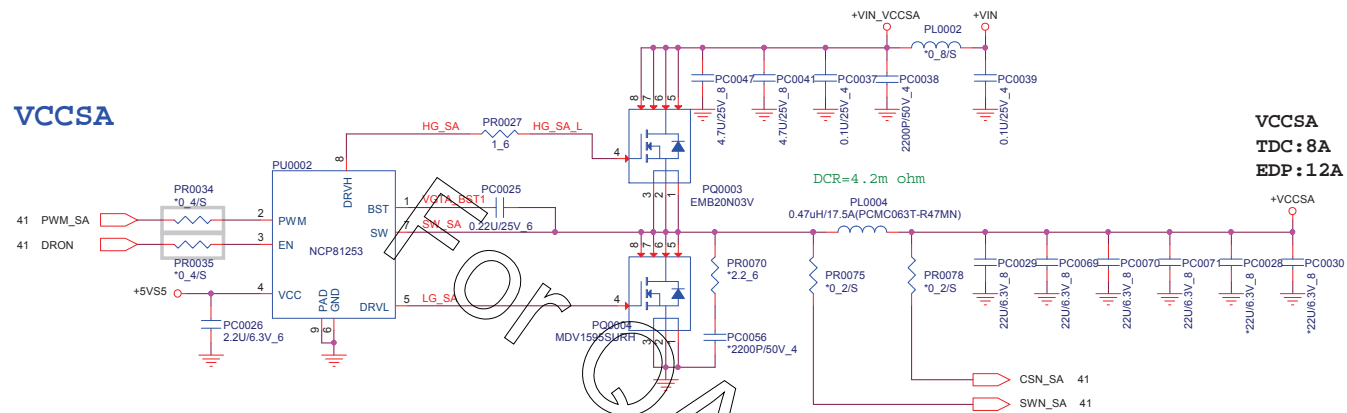


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Quanta Computer Inc.

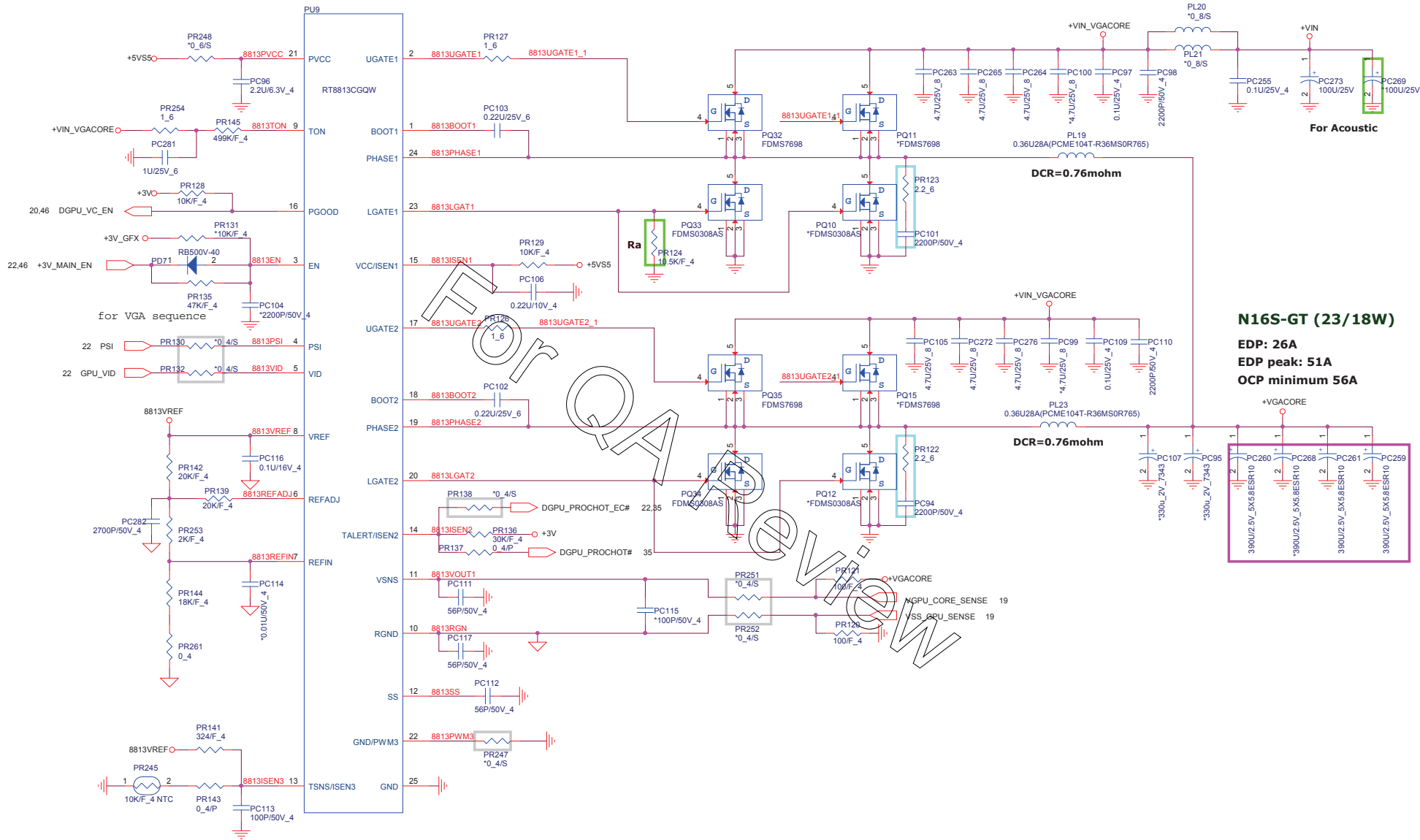
Size Custom	Document Number <b>+1.0V/+VCCSTPLL</b>	Rev 1A
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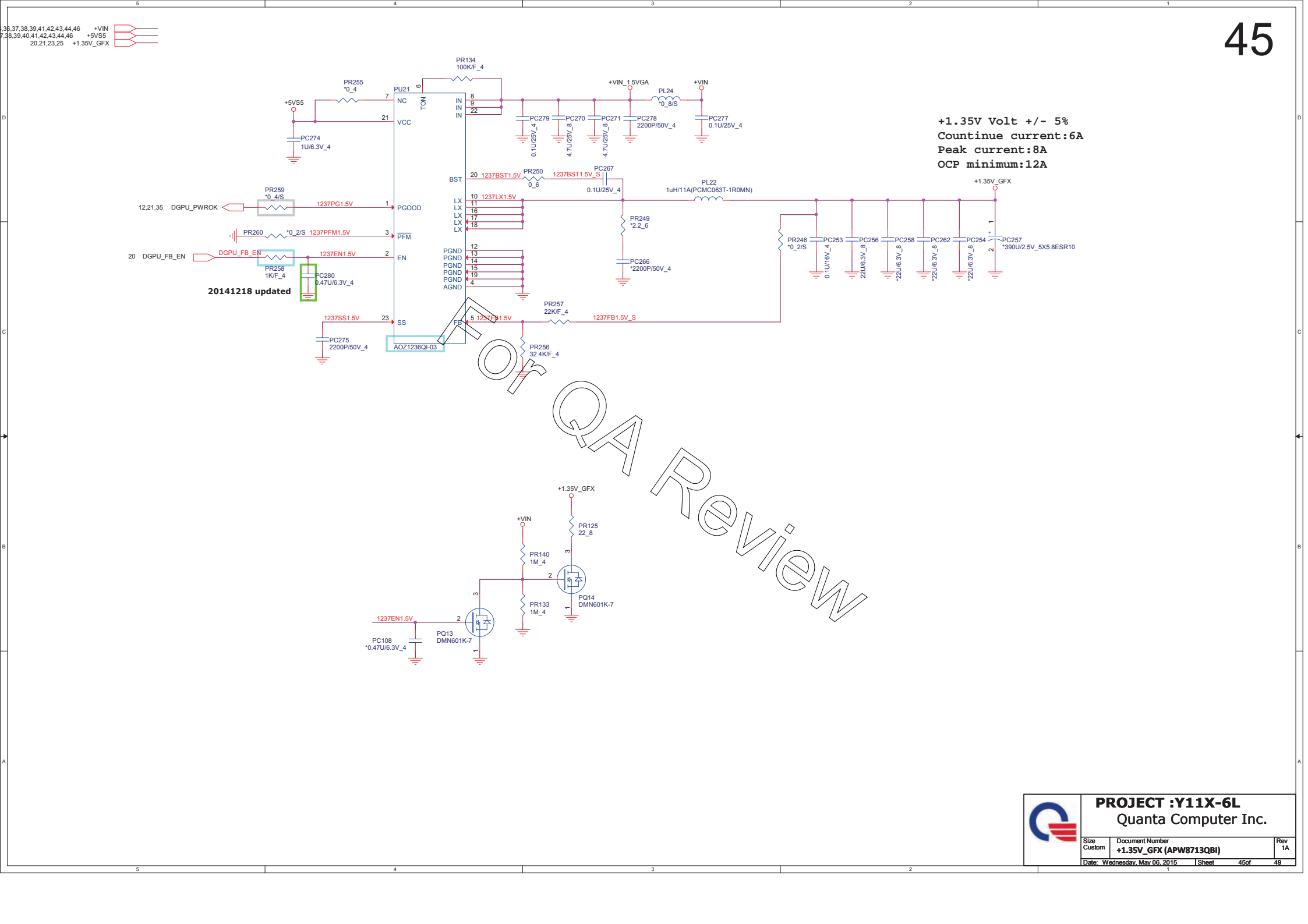




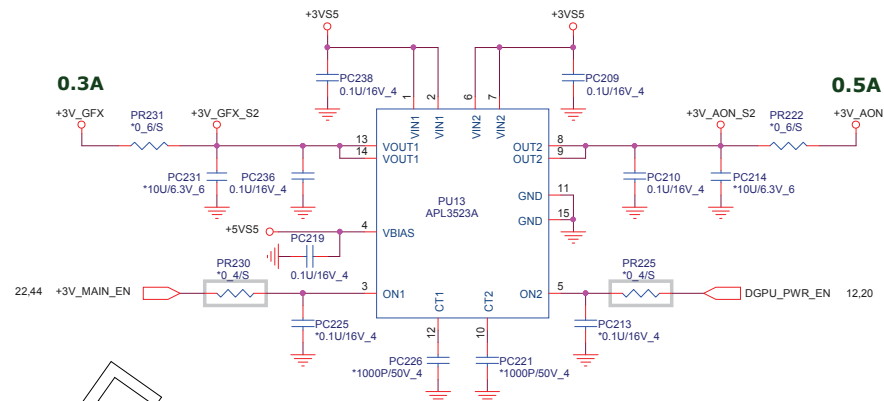
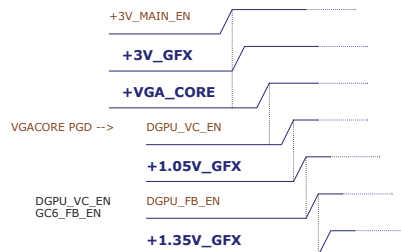


**PROJECT :Y11X-6L**  
**Quanta Computer Inc.**

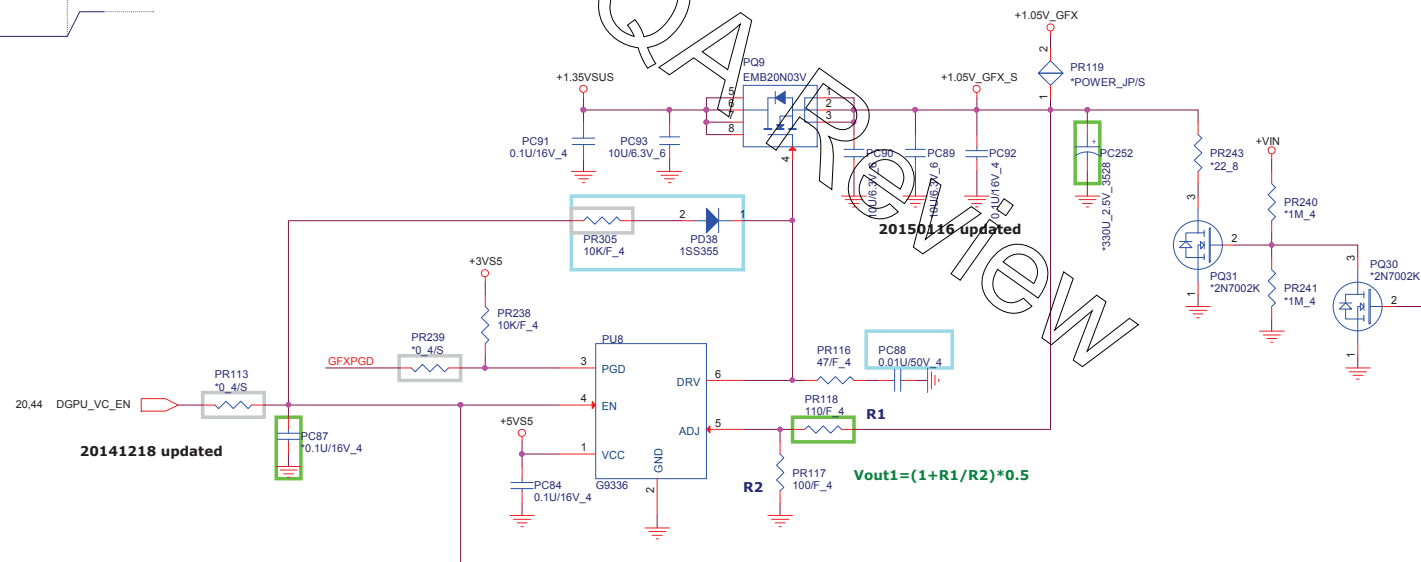
Size Custom	Document Number <b>+VGACORE (RT8813C)</b>	Rev 1A
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28,31,33,34,36,37,38,39,41,42,43,44,45	+VIN
4,10,15,16,32,34,35,37,39,40,43	+3VS5
4,30,32,33,37,38,39,40,41,42,43,44,45	+5VS5
3,6,17,18,38,40	+1.35VSUS
19,21,22,44	+3V_GFX
19,21,22,32	+3V_AON
19,20,21	+1.05V_GFX



**+1.05V\_GFX +/- 5%**  
**Countinue current:0.79A**  
**Peak current:2.09A**



**PROJECT :Y11X-6L**  
**Quanta Computer Inc.**

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